

## Quarterly Technical Report

# Solid State Research

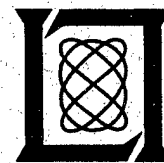
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**Lincoln Laboratory**

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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**SOLID STATE RESEARCH**

**QUARTERLY TECHNICAL REPORT**

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## **ABSTRACT**

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 February through 30 April 1997. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, ARPA, Navy, BMDO, NASA, and NIST.

## TABLE OF CONTENTS

Abstract	iii
List of Illustrations	vii
List of Tables	x
Introduction	xi
Reports on Solid State Research	xiii
Organization	xxi
 1. QUANTUM ELECTRONICS	 1
1.1 Dual-Layer, Optimal Antireflection Coatings for Diode Lasers	1
 2. ELECTRO-OPTICAL MATERIALS AND DEVICES	 7
2.1 High-Quantum-Efficiency GaInAsSb/AlGaAsSb/GaSb Thermophotovoltaic Devices Grown by Organometallic Vapor-Phase Epitaxy	 7
 3. SUBMICROMETER TECHNOLOGY	 13
3.1 Photolithography at 0.11 $\mu\text{m}$ Using ArF Excimer Laser Lithography and Chromeless Phase Shifting Masks	 13
 4. HIGH SPEED ELECTRONICS	 21
4.1 Development of a SiC Vertical Field-Effect Transistor	21
 5. MICROELECTRONICS	 27
5.1 128 $\times$ 128-Pixel CCD Imager with JFET Readout Amplifiers	27
 6. ANALOG DEVICE TECHNOLOGY	 31
6.1 2-GHz Operation of the Digital Control Registers of a Programmable Filter for a Spread-Spectrum Modem	 31
 7. ADVANCED SILICON TECHNOLOGY	 37
7.1 3.2 G-Sample/Second Silicon-on-Insulator CMOS Data Thinner for a Superconductive Compressive Receiver	 37

## LIST OF ILLUSTRATIONS

Figure No.		Page
1-1	Output vs current during typical empirical refinement iteration for large-divergence ( $40^\circ$ full width at half-maximum [FWHM]) diode laser. Curves 1, 2, and 3 show the threshold increasing as increments of the second-layer thickness are added. Curve 4 shows the decrease in threshold after the fourth addition.	3
1-2	Normalized amplified spontaneous emission spectra of large-divergence ( $40^\circ$ FWHM) diode laser showing relatively narrow uncoated gain peak (curve 1). After antireflection (AR) coating one facet (curve 2), the peak broadens and shifts to shorter wavelengths (band filling). Finally, with the obverse side AR coated (curve 3), the broadening is very large and the peak is again shifted further to shorter wavelengths.	4
2-1	External quantum efficiency of thermophotovoltaic (TPV) devices described in Table 2-1.	9
2-2	External quantum efficiency of TPV devices with AlGaAsSb window layer.	9
2-3	Photoluminescence spectra of TPV devices with and without GaSb or AlGaAsSb window layer.	10
3-1	Exposure-defocus plots for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-numerical-aperture (NA), $0.3\text{-}\sigma$ lens. The calculations were repeated four times for four different sets of lens aberrations.	14
3-2	Experimentally measured focus latitude for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-NA, $0.6\text{-}\sigma$ lens. The doses used were $48\text{ mJ/cm}^2$ (open circles), $50\text{ mJ/cm}^2$ (squares), $53\text{ mJ/cm}^2$ (inverted triangles), and $56\text{ mJ/cm}^2$ (closed circles). At a $50\text{-mJ/cm}^2$ dose, the defocus latitude for a nominal 110-nm feature is $\sim 1.5\text{ }\mu\text{m}$ .	16
3-3	Experimentally measured exposure latitude for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-NA, $0.6\text{-}\sigma$ lens. The calculated latitude for $\pm 10\%$ linewidth variation is $\sim 3\%$ for a nominal feature size of 110 nm.	16

## LIST OF ILLUSTRATIONS (Continued)

Figure No.		Page
3-4	Electron micrographs of 110-nm isolated lines produced using chromeless phase edge photomask in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$ lens. The images show the change in feature profile as the spatial period is varied: (a) 270 nm, (b) 250 nm, (c) 240 nm, and (d) 230 nm.	17
3-5	Aerial image calculations showing image placement for 110-nm isolated line vs defocus using four different sets of projection-lens Zernike polynomials. The image was created using a chromeless phase edge. The four lenses are described in Table 3-1.	18
3-6	Electron micrographs of 110-nm isolated lines produced using chromeless phase edge photomask in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$ lens. The images show the change in feature profile as the exposure dose is varied: (a) 49 mJ/cm <sup>2</sup> , (b) 51.5 mJ/cm <sup>2</sup> , (c) 54 mJ/cm <sup>2</sup> , and (d) 58 mJ/cm <sup>2</sup> . Note the decrease in the amount of etch residue as the dose is increased.	19
4-1	Scanning electron micrograph (SEM) of etched-groove grating structure in 6H SiC. The device active area ( $80 \times 16 \mu\text{m} = 4 \text{ mm}$ source width) is indicated by the dashed line.	22
4-2	(a) Simulated and (b) experimental current-voltage (I-V) characteristics obtained for U-groove metal-semiconductor field-effect transistor (MESFET) structure of Figure 4-1, but with drain and source reversed. The top contact for the experimental device is a forward-biased Schottky drain with the substrate as the source.	23
4-3	Characteristics of drain-up MESFET structure of Figure 4-1, but using 4H SiC. The distortions in the I-V curves are due to probe-induced oscillations.	24
4-4	(a) SEM of top ohmic after Ni alloying at 950°C, showing Ni delamination, and (b) SEM showing Ni after alloying at 1050°C but using nitride cap to prevent delamination. Insets show I-V characteristics of top ohmic probed between sets of adjacent fingers.	25
5-1	Optical photograph of the junction field-effect transistor (JFET) source-follower amplifier at end of charge-coupled device (CCD) output register.	27
5-2	(a) Cross-sectional and (b) top views of finished JFET device with surrounding CCD gate electrodes.	28

## LIST OF ILLUSTRATIONS (Continued)

Figure No.		Page
5-3	Average signal vs variance for each pixel in $32 \times 128$ -pixel section of imaging array. The voltage gain and bandwidth for the measured data were 22 and 5 MHz, respectively.	29
6-1	Block diagram of superconductive programmable matched filter.	31
6-2	Filter comprising mainly an array of identical elements, one for each bit in the spreading code: (a) block diagram of element, referred to as a slice; and (b) arrangement of slices to form seven-stage filter. A wire that runs by and couples inductively to each tap serves as a summing bus, whose signal is connected to a quantum flux parametron (QFP) sense circuit.	32
6-3	Layout of top part of prototype test filter, showing three-phase shift register and buffer array that constitute binary reference register.	34
6-4	Layout of analog core section of prototype filter. At the top one sees the buffers of the sampling control register. The T/H elements, with the input signal applied, are seen above and below the taps, with the summing bus connected to the QFP sense comparator.	34
6-5	Waveforms captured during simultaneous operation of both shift registers in filter at 1 GHz with return-to-zero (RZ) input signals. The horizontal scale is 5 ns per division. The top trace shows one phase of the 1-GHz sine wave clocks. The second and third traces show, respectively, the input to and output from the binary reference register, while the bottom two traces show, respectively, the input to and output from the sampling control register.	35
6-6	Waveforms captured during operation of single shift register at 2 GHz using non-return-to-zero input signal produced by combining two 1-GHz RZ channels from the word generator. The horizontal scale is 1 ns per division. The top trace shows one phase of the 2-GHz sine wave clocks. The second and third traces show, respectively, the input to and output from the binary reference register.	36
7-1	Block diagram of digital center-of-pulse (DCOP) test chip.	37
7-2	Metal 1 plot of DCOP test chip.	38

## LIST OF TABLES

Table No.		Page
2-1	GaInAsSb/GaSb Thermophotovoltaic Structures	8
3-1	Lists of Zernike Polynomial Coefficients Used to Simulate Different Lenses for Aerial Image Calculations	14
3-2	Process Conditions for Modified Silylation Resist Processing	15

## INTRODUCTION

### 1. QUANTUM ELECTRONICS

A very simple technique has been developed in the design and fabrication of optimum antireflection (AR) coatings on diode lasers, which bypasses complex modeling and calculation of the modal properties of the optical waveguide. By modifying conventional AR coating designs by folding in decomposed far-field intensity data and following with empirical refinement, effective reflectivities in the range  $10^{-3}$ – $10^{-4}$  can be routinely achieved, and external cavity diode lasers with the applied AR coatings have resulted in 5% tuning ranges, mode suppression of –50 dB, and calculated modal reflectivities as low as  $4 \times 10^{-5}$ .

### 2. ELECTRO-OPTICAL MATERIALS AND DEVICES

Lattice-matched GaInAsSb/AlGaAsSb/GaSb thermophotovoltaic devices with cutoff wavelengths of  $2.2 \mu\text{m}$  have demonstrated external quantum efficiency as high as 55% and open circuit voltage of 290 mV. The use of an AlGaAsSb window layer reduces surface recombination and results in improved performance compared to devices without a window layer.

### 3. SUBMICROMETER TECHNOLOGY

ArF (193-nm wavelength) excimer laser lithography has been evaluated for the fabrication of 0.11- $\mu\text{m}$ -wide features using chromeless phase shifting masks. Good resolution and depth of focus have been demonstrated, but image distortion effects have been identified that may limit the useful depth of focus.

### 4. HIGH SPEED ELECTRONICS

A submicrometer-periodicity vertical metal-semiconductor field-effect transistor has been developed in SiC, and the technology necessary to fabricate it in this material has been demonstrated. This device coupled with the material properties of SiC should enable unprecedented power-frequency performance from L-band to X-band frequencies.

### 5. MICROELECTRONICS

A *p*-channel junction field-effect transistor (JFET), fabricated in a selectively grown single-crystal silicon layer, has been integrated onto a  $128 \times 128$ -pixel charge-coupled device (CCD) imager. The JFET devices, used in the charge readout amplifier, are being developed to convert the CCD electron packets into a usable voltage while adding negligible noise.

### 6. ANALOG DEVICE TECHNOLOGY

High-speed tests have been performed on the digital control registers of a programmable filter for a very high speed direct-sequence spread-spectrum modem based on niobium Josephson-junction technol-

ogy. The filter, using mixed analog-digital circuitry, is designed to demodulate 2-gigachip-per-second direct-sequence-encoded spread-spectrum signals and features burst-synchronization capability, that is, the ability to determine within just a few signal bits the timing offset between the codes in the transmitter and receiver.

## **7. ADVANCED SILICON TECHNOLOGY**

The digital center-of-pulse (DCOP) test chip has been designed to perform the high-speed (800-MHz clock) operations of a data thinner for Lincoln Laboratory's superconducting compressive receiver. The chip, comprising about 22 000 transistors, is being fabricated at Lincoln Laboratory in a fully depleted silicon-on-insulator CMOS process with 0.25- $\mu\text{m}$  transistor gates.

## REPORTS ON SOLID STATE RESEARCH

1 FEBRUARY THROUGH 30 APRIL 1997

### PUBLICATIONS

Photoresists for 193-nm Lithography	R. D. Allen* G. M. Wallraff* D. C. Hofer* R. R. Kunz	<i>IBM J. Res. Develop.</i> <b>41</b> , 95 (1997)
Self-Aligned Pseudomorphic HEMT with a Low-Temperature-Grown GaAs Gate Insulator	C. L. Chen L. J. Mahoney S. D. Calawa K. M. Molvar A. R. Calawa	<i>Electron. Lett.</i> <b>33</b> , 640 (1997)
Mid Infrared Semiconductor Lasers	H. K. Choi	<i>Laser Rev.</i> <b>25</b> , 9 (1997)
Can Advanced Photoresists Extend Optical Lithography?	R. R. Kunz	<i>Semicond. Int.</i> <b>20</b> (2), 86 (1997)
Simple Compact Diode-Laser/Microlens Packaging	Z. L. Liao D. Z. Tsang* J. N. Walpole	<i>IEEE J. Quantum Electron.</i> <b>33</b> , 457 (1997)
Lithography at a Wavelength of 193 nm	M. Rothschild A. R. Forte R. R. Kunz S. C. Palmateer J. H. C. Sedlacek	<i>IBM J. Res. Develop.</i> <b>41</b> , 49 (1997)
Thin-Film Imaging: Past, Present, Prognosis	D. E. Seeder* D. C. LaTulipe, Jr.* R. R. Kunz C. M. Garza* M. A. Hanratty*	<i>IBM J. Res. Develop.</i> <b>41</b> , 105 (1997)

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\* Author not at Lincoln Laboratory.

Binary Optics: A VLSI-Based Microoptics Technology	M. B. Stern	<i>Microelectron. Eng.</i> <b>32</b> , 369 (1996)
GaInAsSb/AlGaAsSb Multiple-Quantum-Well Diode Lasers Grown by Organometallic Vapor Phase Epitaxy	C. A. Wang H. K. Choi	<i>Appl. Phys. Lett.</i> <b>70</b> , 802 (1997)
Characteristics of GaSb Growth Using Various Gallium and Antimony Precursors	C. A. Wang S. Salim* K. F. Jensen* A. C. Jones*	<i>J. Cryst. Growth</i> <b>170</b> , 55 (1997)
Periodically Poled Lithium Niobate Optical Parametric Amplifiers Pumped by High-Power Passively <i>Q</i> -Switched Microchip Lasers	J. J. Zayhowski	<i>Opt. Lett.</i> <b>22</b> , 169 (1997)
Miniature Solid-State Lasers	J. J. Zayhowski J. Harrison*	In <i>CRC Handbook of Photonics</i> , M. C. Gupta, ed. (CRC Press, Boca Raton, Fla., 1996), p. 326

#### ACCEPTED FOR PUBLICATION

Resonant-Tunneling Transmission-Line Relaxation Oscillator	E. R. Brown C. D. Parker S. Verghese M. W. Geis J. F. Harvey*	<i>Appl. Phys. Lett</i>
Soft-X-Ray CCD Imagers for AXAF	B. E. Burke J. A. Gregory M. W. Bautz* G. Y. Prigozhin* S. R. Kissel* B. B. Kosicki A. H. Loomis D. J. Young	<i>IEEE Trans. Electron Devices</i>

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\* Author not at Lincoln Laboratory.

Frequency Tunable Microstrip Resonator in the Partially Magnetized State	G. F. Dionne D. E. Oates	<i>IEEE Trans. Magn.</i>
Hole Traps in Natural Type IIB Diamond	M. W. Geis J. C. Twichell	<i>IEEE Trans. Electron Devices</i>
Three-Dimensional Metallodielectric Photonic Crystals Exhibiting Resonant Infrared Stop-Bands	K. A. McIntosh L. J. Mahoney K. M. Molvar O. B. McMahon S. Verghese M. Rothschild E. R. Brown	<i>Appl. Phys. Lett</i>
Critical-State Model for Harmonic Generation in a Superconducting Microwave Resonator	D. E. Oates J. MacDonald* J. R. Clem*	<i>Phys. Rev. B</i>
OMVPE Growth of GaInAsSb/AlGaAsSb for Quantum-Well Diode Lasers	C. A. Wang H. K. Choi	<i>J. Electron. Mater.</i>
Microchip Optical Parametric Oscillators	J. J. Zayhowski	<i>Opt. Lett.</i>

### PRESENTATIONS<sup>†</sup>

The Orthogonal-Transfer CCD	B. E. Burke J. L. Tonry*	SPIE Symposium on Electronic Imaging '97, San Jose, California, 8-14 February 1997
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<sup>†</sup> Titles of presentations are listed for information only. No copies are available for distribution.

External Cavity Mid-Infrared  
Semiconductor Lasers

H. Q. Le  
G. W. Turner  
J. R. Ochoa  
M. J. Manfra  
C. C. Cook  
Y.-H. Zhang\*

Photonics West '97,  
San Jose, California,  
8-14 February 1997

High-Power 1.3  $\mu\text{m}$  InGaAsP/InP  
Lasers and Amplifiers with Tapered  
Gain Regions

J. N. Walpole  
G. E. Betts  
J. P. Donnelly

Optoelectronics '97: Integrated  
Devices and Applications,  
San Jose, California,  
8-14 February 1997

GaInAsSb/AlGaAsSb Diode Lasers  
Grown by Organometallic Vapor Phase  
Epitaxy

C. A. Wang  
H. K. Choi

Noise and Gain Measurements of High-  
Power 1.3  $\mu\text{m}$  InGaAsP/InP Tapered  
Amplifiers

G. E. Betts  
J. P. Donnelly  
J. N. Walpole  
S. H. Groves  
F. J. O'Donnell  
L. J. Missaggia  
R. J. Bailey  
A. Napoleone

Optical Fiber  
Communications '97,  
Dallas, Texas,  
16-21 February 1997

Overview of GaSb-Based Materials  
Research at MIT Lincoln Laboratory

G. W. Turner  
H. K. Choi  
M. J. Manfra  
M. K. Connors

Lincoln Laboratory  
Technical Seminar Series,  
University of Pittsburgh,  
Pittsburgh, Pennsylvania,  
17 February 1997

A Deep Submicrometer Fully Depleted  
Low Power SOI CMOS Process  
Technology

J. A. Burns

Lincoln Laboratory  
Technical Seminar Series,  
University of California  
at Berkeley,  
Berkeley, California,  
21 February 1997

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Trends in Photolithography	D. K. Astolfi	Meeting of the New England Chapter of the Semiconductor Safety Association, Lexington, Massachusetts, 26 February 1997
High Power High Brightness Optically Pumped Mid-Infrared Semiconductor Lasers and Applications	H. Q. Le	Lincoln Laboratory Technical Seminar Series, Arizona State University, Tempe, Arizona, 27 February 1997; University of Connecticut, Storrs, Connecticut, 25 April 1997
Deep-Submicrometer SOI CMOS Using Advanced Optical Lithography	C. L. Keast	VLSI Seminar Series, Massachusetts Institute of Technology, Cambridge, Massachusetts, 4 March 1997
Bio-aerosol Fluorescence Sensor	T. H. Jeys S. DiCecca G. S. Rowe N. R. Newbury A. Sanchez C. Primmerman F. Reyes*	1997 Meeting of the Infrared Information Symposia Group on Active Systems, Tucson, Arizona, 5-7 March 1997

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Positive, Chemically Amplified, Silylated Resists for 193 nm Lithography	J. R. Bohland* G. N. Taylor* A. R. Forte S. C. Palmateer	SPE Symposium on Microlithography '97, Santa Clara, California, 9-14 March 1997
Performance of Excimer Lasers as Light Sources for 193-nm Lithography	J. H. C. Sedlacek S. P. Doran M. Fritze R. R. Kunz M. Rothschild R. Uttaro	
Sub-0.25 $\mu\text{m}$ Fully Depleted SOI CMOS Process for Low Power, High Performance Applications	C. L. Keast A. M. Soares R. Berger D. C. Shaver J. A. Burns J. M. Knecht R. R. Kunz H. I. Liu P. W. Wyatt	1997 Government Microcircuit Applications Conference, Las Vegas, Nevada, 13 March 1997
Practical Implementation of a Top Surface Imaging Silylation Resist into Device Fabrication at 193 nm	A. R. Forte	Technical Seminar, LAM Research Corp., Santa Clara, California, 14 March 1997
Infrared Metallodielectric Photonic Crystals	K. A. McIntosh L. J. Mahoney K. M. Molvar O. B. McMahon	Optical Society of America Spring Topical Meetings, Incline Village, Nevada, 17-21 March 1997
Fiber-Coupled Photomixers Operating at Cryogenic Temperatures	S. Verghese K. A. McIntosh E. R. Brown	

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Diamond Surface Emission Cathodes	M. W. Geis N. N. Efremow K. E. Krohn J. C. Twichell T. M. Lyszczarz	1996 ARPA High Definition Systems Information Exchange Conference, Arlington, Virginia, 23-26 March 1997
Integrated Optical Guided-Wave Components and Devices in AlGaAs/GaAs and InGaAsP/InP	J. P. Donnelly	Lincoln Laboratory Technical Seminar Series, Worcester Polytechnic Institute, Worcester, Massachusetts, 24 March 1997
Laser Micromachining of Silicon: A New Technique for Fabricating High Quality Terahertz Waveguide Components	C. K. Walker* T. M. Bloomstein S. T. Palmacci M. B. Stern J. E. Curtin	8th International Symposium on Space Terahertz Technology, Cambridge, Massachusetts, 25-27 March 1997
Prospects for High Thermoelectric Figures of Merit in 2D Systems	M. S. Dresselhaus* T. C. Harman X. Sun* S. B. Cronin* K. L. Wang*	1997 Spring Meeting of the Materials Research Society, San Francisco, California, 31 March-4 April 1997
High Thermoelectric Figures of Merit in PbTe Quantum Wells	T. C. Harman D. L. Spears M. P. Walsh X. Sun* S. B. Cronin* M. S. Dresselhaus*	
Characterization and Chemical Etching of the Thermally Grown Oxide on GaN	R. Molnar	
The Hydride Vapor Phase Epitaxial Growth of GaN Films for Quasi-Bulk Substrates	R. Molnar	

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Frequency Tunable Microstrip Resonator in the Partially Magnetized State	G. F. Dionne D. E. Oates	Intermag '97 New Orleans, Louisiana, 1-4 April 1997
OMVPE Growth of GaInAsSb/AlGaAsSb for Quantum-Well Diode Lasers	C. A. Wang H. K. Choi	8th Biennial Workshop on Organometallic Vapor Phase Epitaxy, Dana Point, California, 13-17 April 1997
MIT Lincoln Laboratory's Microelectronics Laboratory	C. L. Keast	Lincoln Laboratory Technical Seminar Series, Northwestern University, Chicago, Illinois, 14 April 1997
Solid State Laser Development at Lincoln Laboratory	T. Y. Fan	Technical University Vienna, Vienna, Austria, 23 April 1997
Superconductive Passive Microwave Devices	W. G. Lyons	Lincoln Laboratory Technical Seminar Series, University of Michigan, Ann Arbor, Michigan, 24 April 1997
Microchip Lasers	J. J. Zayhowski	Lincoln Laboratory Technical Seminar Series, Tufts University, Medford, Massachusetts, 28 April 1997

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## ADVANCED SILICON TECHNOLOGY

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# 1. QUANTUM ELECTRONICS

## 1.1 DUAL-LAYER, OPTIMAL ANTIREFLECTION COATINGS FOR DIODE LASERS

Antireflection (AR) coatings on the facets of semiconductor lasers have been of great interest since at least 1973 [1]. Currently, the practical goal for AR coatings applied to external cavity lasers and traveling-wave amplifiers is a residual reflectivity in the  $10^{-3}$ – $10^{-4}$  range or less [2]–[5]. The difficulty in determining the optimum coating parameters arise from the non-plane wave nature of the light emitted from the optical waveguide and the complexity involved in calculating the effective modal refractive index of the cavity. Many techniques for modeling the waveguide and calculating the optimal coating parameters have relied on approximations such as neglecting the waveguide altogether (approximating the cavity by a constant index [6]–[8]) or using an ad hoc Fourier approach (assuming gaussian fields and/or single propagating TE mode) [4],[9],[10]. Other more rigorous methods have also been presented considering both TE and TM modes, but often rely on other approximations or simplifications such as weakly guided structures [2],[11]–[13]. Here, we present a method for determination of optimal dual-layer AR coating parameters for diode lasers. This method sidesteps modeling of the optical waveguide in exchange for an empirical refinement step which is somewhat labor intensive but potentially offers a truly practical technique for the fabrication of lowest-modal-reflectivity AR coatings for a given device structure and set of coating materials.

Our recipe for the development of optimal diode laser AR coatings consists of four main steps: (1) Design the initial dual-layer coating in a conventional manner (single plane wave) assuming a reasonable guess at the modal refractive index. (2) Determine if modification of the design is necessary by decomposing the gaussian beam into a set of  $N$  plane waves propagating with different intensity weighted k-vectors and seeing if the calculated modal reflectivity falls within the  $10^{-4}$  range. (3) If it does not fall within the range, then modify the AR coating design utilizing the decomposed beam in a computer-based optimization program. (4) Empirically refine the AR coating design in the fabrication phase by making small changes in the layers until the post-process performance of the device is optimized.

Given the far-field pattern of a laser diode, the distribution can be deconvolved into plane waves of different k-vectors to approximate the output of the laser (although a near-field distribution gives a more exact picture) [10]. Each plane wave is weighted with a factor proportional to its related intensity. The accurate description of intensity weight involves an integral over the distribution of plane waves, but for an approximate calculation the integral becomes a sum:

$$\text{WFactor}_i = \frac{I(\theta_i)\Delta\theta}{\sum_{i=1}^N I(\theta_i)\Delta\theta} , \quad (1.1)$$

where  $\text{WFactor}_i$  is the intensity weight of the  $i$ th plane wave. The modal power reflectivity may then be approximated:

$$R_{\text{eff}} = \sum_{i=1}^N R(\theta_i + \Delta\theta/2) \text{WFactor}_i, \quad (1.2)$$

where  $R$  for the case of the dual-layer coating ( $R \ll 1$ ) at each angle is given by [14]

$$R(\theta) = \left\{ \frac{4n_0n_s}{\left[ (n_0 - n_s)A - \left( \frac{n_0n_2}{n_1} - \frac{n_sn_1}{n_2} \right)B \right]^2 + \left[ \left( n_1 - \frac{n_0n_s}{n_1} \right)C - \left( n_2 - \frac{n_0n_s}{n_2} \right)D \right]^2} \right\}^{-1}, \quad (1.3)$$

where  $A = \cos \delta_1 \cos \delta_2$ ,  $B = \sin \delta_1 \sin \delta_2$ ,  $C = \sin \delta_1 \cos \delta_2$ ,  $D = \cos \delta_1 \sin \delta_2$ ,  $\delta_1 = 2\pi n_1 d_1 \cos \theta_1 / \lambda$ , and  $\delta_2 = 2\pi n_2 d_2 \cos \theta_2 / \lambda$ . The incident medium index is  $n_0$ , the substrate index is  $n_s$ , and the refractive indexes of the two-layer coating are  $n_1$  and  $n_2$ , with the thicknesses likewise defined by  $d_1$  and  $d_2$ . The angles  $\theta_1$ ,  $\theta_2$  are related to the far-field angles  $\theta_i$  through Snell's law.

If it is found that the initial AR design needs modification, i.e., if calculation of Equation (1.2) is outside the  $10^{-4}$  range, then the design is optimized by varying the layer thickness and effectively minimizing  $R_{\text{eff}}$ .

The dual-layer AR coatings are fabricated in a Balzers BAK640 coating machine by standard electron-beam evaporation at ambient substrate temperatures. The coating materials, procedures, and parameters are chosen to be consistent with the coating of semiconductor device structures. The end point of the coating layers is determined optically by monitoring the reflection from a single undoped GaAs witness substrate roughened on the obverse side.

Evaluation of the witness sample is accomplished in reflection utilizing a Perkin-Elmer Lambda-9 with a standard  $5^\circ$  off-normal reflectance accessory.

Threshold plots of diodes coated with this technique are shown in Figure 1-1. Curves 1, 2, and 3 show the threshold increasing as increments of the second-layer thickness are added. Curve 4 shows the decrease in threshold after the fourth addition. The increase in threshold current at the optimum second-layer thickness (curve 3) is seen to be three to four times that of the uncoated laser. The devices depicted by these curves had a large divergence, about  $40^\circ$  full width at half-maximum (FWHM), so it was expected from our calculation using Equation (1.2) that the effective reflectivity of the refined coating could be no better than the  $10^{-3}$  range. In contrast, optimized AR coatings on devices with smaller divergence,  $30^\circ$  FWHM or less, were seen to have threshold in excess of 8 times the uncoated threshold, with the threshold of some shorter-cavity devices being indeterminable because of roll-off in the gain as a function of current density. Significant gain roll-off can seriously limit the effective application of this technique in the case of short cavity lengths ( $\sim 0.5$  mm or less) [15].

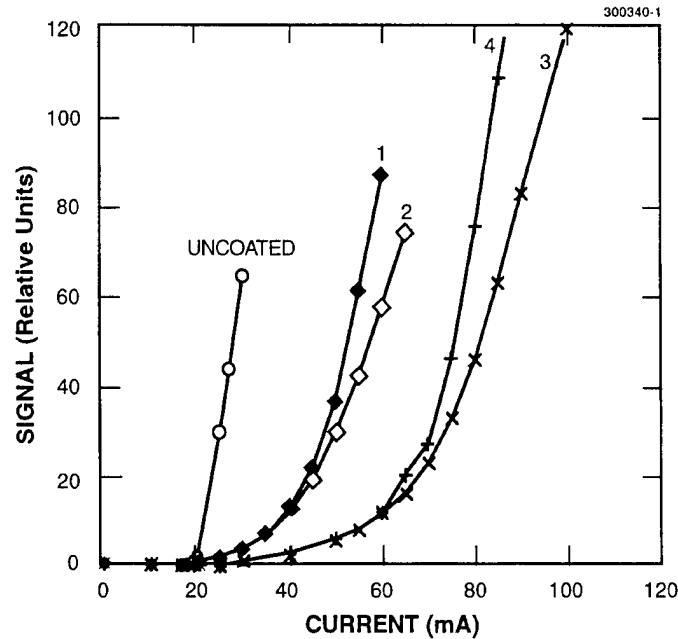


Figure 1-1. Output vs current during typical empirical refinement iteration for large-divergence ( $40^\circ$  full width at half-maximum [FWHM]) diode laser. Curves 1, 2, and 3 show the threshold increasing as increments of the second-layer thickness are added. Curve 4 shows the decrease in threshold after the fourth addition.

The amplified spontaneous emission (ASE) spectra for a diode laser used as a traveling-wave amplifier is shown in Figure 1-2 (also large divergence). The Fabry-Perot modes of the cavity did not need to be resolved for this evaluation. As can be seen, there is a large shift ( $\sim 25$  nm) in the position of the gain peak upon AR coating just one facet (curve 2; curve 1 is the uncoated ASE). With an additional AR coating on the obverse side (curve 3) the peak shifts about another 15 nm. In order for the AR coatings on an amplifier to be optimal, knowledge of the expected shifts must be known, and a correction must be made to the design. It is of interest to note that the rather large divergence of these lasers resulted in the largest modifications and refinements. This makes sense because the phase thickness of the coating layers as well as the effective index of the waveguide vary as  $\delta, n_s \propto \cos \theta$ , which leads to an increasing correction at half angles above  $15^\circ$  ( $30^\circ$  full width).

AR coatings applied to diode lasers (InGaAsP, multiple quantum well, separate confinement heterostructure) emitting around  $\lambda = 1.55 \mu\text{m}$  with angular distributions less than  $30^\circ$  using our technique have resulted in calculated effective reflectivities as low as  $4 \times 10^{-5}$ . When used in external cavities, the lasers showed a large tuning range of 1505–1580 nm with a mode suppression ratio as low as  $-50$  dB [16].

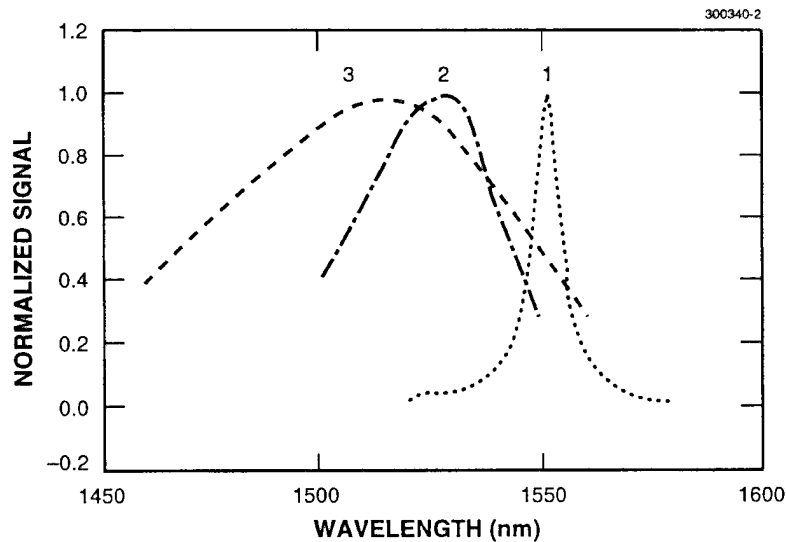


Figure 1-2. Normalized amplified spontaneous emission spectra of large-divergence ( $40^\circ$  FWHM) diode laser showing relatively narrow uncoated gain peak (curve 1). After antireflection (AR) coating one facet (curve 2), the peak broadens and shifts to shorter wavelengths (band filling). Finally, with the obverse side AR coated (curve 3), the broadening is very large and the peak is again shifted further to shorter wavelengths.

The technique developed for device-driven optimization has successfully met our goals of diode laser AR coatings in the range  $10^{-3}$ – $10^{-4}$ , even under the rather less than ideal coating conditions required to fabricate them on packaged devices. These conditions result in rather porous coatings that tend to shift spectrally upon exposure to the atmosphere. Although the technique described allows for the relatively repeatable correction for this shift, improvements will include using ion-assisted deposition to produce nonporous coatings and eliminate possible problems with inhomogeneity.

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## 2. ELECTRO-OPTICAL MATERIALS AND DEVICES

### 2.1 HIGH-QUANTUM-EFFICIENCY GaInAsSb/AlGaAsSb/GaSb THERMOPHOTOVOLTAIC DEVICES GROWN BY ORGANOMETALLIC VAPOR-PHASE EPITAXY

Recent developments in thermophotovoltaic (TPV) systems are based on thermal sources which operate in the temperature range 1100–1500 K [1]. For high conversion efficiency, the cutoff wavelength of the photovoltaic cell should closely match the peak in emissive power of the thermal source, which for this temperature range corresponds to 1.9–2.6  $\mu\text{m}$ . The GaInAsSb alloys lattice matched to GaSb substrates are of particular interest for TPV systems. Recently, GaInAsSb TPV devices grown by liquid-phase epitaxy and molecular-beam epitaxy have been demonstrated, and external quantum efficiency (QE) exceeding 40% at 2  $\mu\text{m}$  has been obtained [2]–[4]. Here, we report external QE as high as 55% at 2  $\mu\text{m}$  for GaInAsSb devices grown by organometallic vapor-phase epitaxy. These devices include an AlGaAsSb window layer which effectively reduces the surface recombination velocity.

GaInAsSb and AlGaAsSb epitaxial layers were grown on (100) GaSb substrates, oriented  $2^\circ$  toward (110) or  $6^\circ$  toward (111)B, in a vertical rotating-disk reactor operating at 150 Torr with  $\text{H}_2$  as the carrier gas. GaInAsSb layers were grown with triethylgallium (TEGa), trimethylindium, tertiarybutylarsine (TBAs), and trimethylantimony (TMSb); and AlGaAsSb layers with tritertiarybutylaluminum, TEGa, TBAs, and TMSb, as previously reported [5],[6]. Diethyltellurium (50 ppm in  $\text{H}_2$ ) and dimethylzinc (1000 ppm in  $\text{H}_2$ ) were used as the  $n$ - and  $p$ -type doping sources, respectively. All layers were grown lattice matched to GaSb substrates at 550 or 575°C. The growth rate of GaInAsSb was typically 0.7 nm/s, while that of AlGaAsSb was 0.4 nm/s.

Several different TPV structures were grown for comparison. The basic structure consists of an  $n\text{-Ga}_{0.86}\text{In}_{0.14}\text{As}_{0.12}\text{Sb}_{0.88}$  base layer and  $p\text{-Ga}_{0.86}\text{In}_{0.14}\text{As}_{0.12}\text{Sb}_{0.88}$  emitter layer grown lattice matched to a GaSb substrate. Changes to the structure included a variation in base/emitter layer thicknesses and incorporation of an  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}_{0.02}\text{Sb}_{0.98}$  or GaSb window layer. Table 2-1 summarizes the device structures, substrate orientation, 300-K photoluminescence (PL) peak emission, and lattice mismatch  $\Delta a/a$ . The doping level of the  $p\text{-GaInAsSb}$  emitter layer was  $\sim 2 \times 10^{17} \text{ cm}^{-3}$ , while the  $n\text{-GaInAsSb}$  base layer was  $\sim 5 \times 10^{17} \text{ cm}^{-3}$ .

Mesa diodes, 0.5 and 1  $\text{cm}^2$ , were fabricated by a conventional photolithographic process. A single 1-mm-wide central busbar connected to 10- $\mu\text{m}$ -wide grid lines spaced 100  $\mu\text{m}$  apart was used to make electrical contact to the front surface. Ohmic contacts to  $p$ - and  $n\text{-GaSb}$  were formed by depositing Ti/Pt/Au and Au/Sn/Ti/Pt/Au, respectively, and alloying at 300°C. Mesas were formed by wet chemical etching to a depth of 5  $\mu\text{m}$ . No antireflection coatings were deposited on these test devices.

The external QE as a function of wavelength for devices 379, 459, 462, and 463 are shown in Figure 2-1. The value of  $\Delta a/a$  of these structures is  $< 2 \times 10^{-3}$ . A higher QE near the bandedge is observed for 463 with a 3- $\mu\text{m}$ -thick emitter layer and 1- $\mu\text{m}$ -thick base layer, compared to 462 with a 1- $\mu\text{m}$ -thick emitter layer and 3- $\mu\text{m}$ -thick base layer, which likely results because of the higher minority carrier diffusion length in  $p$ -type GaInAsSb compared to  $n$ -type GaInAsSb. However, at shorter wavelengths, the QE of 463

**TABLE 2-1**  
**GaInAsSb/GaSb Thermophotovoltaic Structures**

Wafer	Base ( $\mu\text{m}$ )	Emitter ( $\mu\text{m}$ )	AlGaAsSb ( $\mu\text{m}$ )	GaSb ( $\mu\text{m}$ )	Misorientation	300-K PL ( $\mu\text{m}$ )	$\Delta a/a$ ( $\times 10^{-3}$ )
379*	3	0.2	0	0.05	2-(110)	2.15	0
459*	3	1	0	0	2-(110)	2.24	2
462*	3	1	0	0	6-(111)B	2.24	1
463*	1	3	0	0	6-(111)B	2.24	1.5
542*	1	3	0.1	0.025	6-(111)B	2.26	5
543*	1	3	0.1	0.025	6-(111)B	2.26	2.5
548*	1	3	0.1	0.025	6-(111)B	2.26	-1.2
041†	1	3	0	0	0	2.14	1
068†	1	3	0.1	0.025	0	2.2	0.4
*Grown by organometallic vapor-phase epitaxy.							
†Grown by molecular-beam epitaxy.							

is lower than 462, which consists of a 1- $\mu\text{m}$ -thick emitter layer and 3- $\mu\text{m}$ -thick base layer. Since carriers are predominantly generated in the base layer for 462, this result suggests that these GaInAsSb devices are highly susceptible to surface recombination. The highest QE at wavelengths below 1.6  $\mu\text{m}$  is measured for 379, which has a GaSb window layer. In general, the performance of devices grown on (100) 6° toward (111)B is better than those grown on (100) 2° toward (110).

Figure 2-2 shows the QE as a function of wavelength for 544 and 548, which consist of a 3- $\mu\text{m}$ -thick emitter layer, 1- $\mu\text{m}$ -thick base layer, and nominally lattice-matched  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}_{0.02}\text{Sb}_{0.98}/\text{GaSb}$  window layer. Higher-bandgap window layers are often incorporated to improve the performance of solar cells [7],[8]. The QE of these devices is about 1.5 times higher than devices with a similar structure without the window layer (463), higher than has been previously reported for GaInAsSb/GaSb TPV devices [2]–[4], and approaching the ~70% limit for uncoated devices. The QE is comparable to lattice-mismatched InGaAs/InP devices, which had a maximum QE of nearly 60% at 1.65  $\mu\text{m}$  and dropped off to 20% at 2.2  $\mu\text{m}$  [9]. The value of the open circuit voltage  $V_{\text{oc}}$  is 290 mV at a short circuit current  $I_{\text{sc}}$  of 1 A/cm<sup>2</sup>. This value is similar to that measured for lattice-mismatched InGaAs/InP devices.

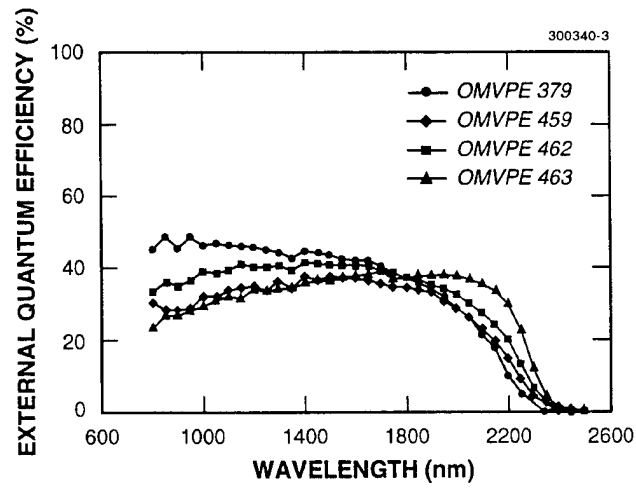


Figure 2-1. External quantum efficiency of thermophotovoltaic (TPV) devices described in Table 2-1.

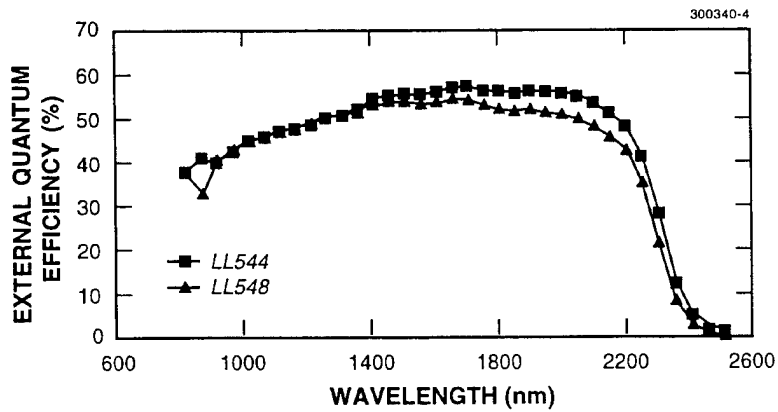


Figure 2-2. External quantum efficiency of TPV devices with AlGaAsSb window layer.

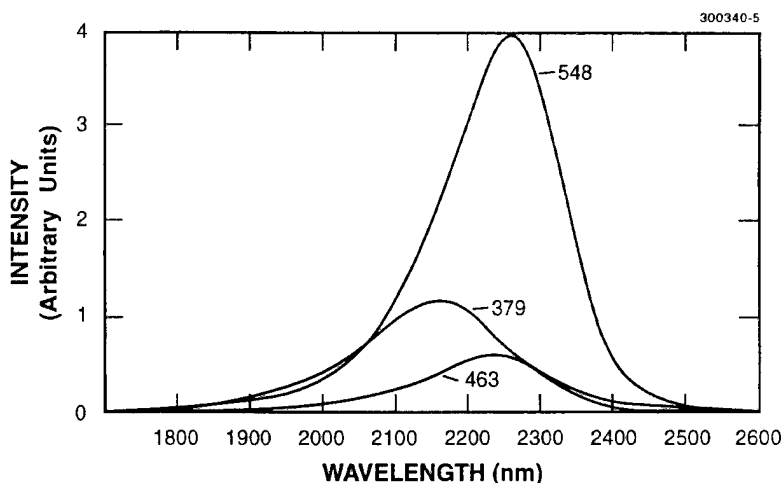


Figure 2-3. Photoluminescence spectra of TPV devices with and without GaSb or AlGaAsSb window layer.

The 300-K PL spectra of TPV structures without a window layer (463) and with a GaSb (379) or AlGaAsSb (548) window layer are shown in Figure 2-3. The PL efficiency for 548 with the AlGaAsSb window layer is about 3.5 times the value for 379 and 7 times higher than 379. Since carriers are generated near the surface in these PL experiments (excitation source is 647 nm), these results indicate that the AlGaAsSb effectively passivates the surface of the underlying GaInAsSb and reduces the surface recombination velocity. Furthermore, standard calculations [10] of external QE suggest that the surface recombination velocity may be reduced by over an order of magnitude with the AlGaAsSb window layer, and that the minority electron diffusion length in our lattice-matched GaInAsSb is about 5  $\mu\text{m}$ . Further characterization of GaInAsSb/AlGaAsSb/GaSb devices should be performed to assess the potential of this materials system for TPV systems.

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### 3. SUBMICROMETER TECHNOLOGY

#### 3.1 PHOTOLITHOGRAPHY AT 0.11 $\mu\text{m}$ USING ArF EXCIMER LASER LITHOGRAPHY AND CHROMELESS PHASE SHIFTING MASKS

The drive to develop lithographic patterning technologies able to produce linewidths at 130 and 100 nm has led to the exploration of techniques to extend traditional optical lithography. It has previously been established [1] that chromeless phase shifting masks can provide the greatest degree of resolution enhancement over conventional binary masks. When this approach is used with low ( $\sim 0.3$ ) partial coherence, high image contrast and depth of field can be achieved with resolution approaching the Rayleigh limit:

$$\text{Resolution} = \lambda / (4 \text{ NA}) \quad , \quad (3.1)$$

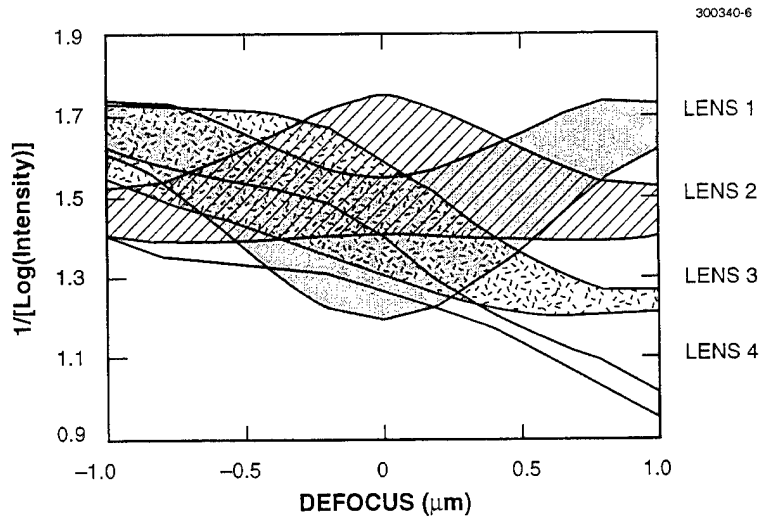
where  $\lambda$  is the exposure wavelength, and NA is the numerical aperture of the optical system. With the absence of chrome lines on the mask to define feature width, other techniques must be used to control line-width. In principle, the critical dimension of features created with this method can be controlled through means of varying the numerical aperture and/or the partial coherence. Feature size decreases with increasing numerical aperture and decreasing partial coherence ( $\sigma$ ). The exposure latitude is reduced with increasing partial coherence as a result of the poorer image contrast, but this trade-off does not exist for critical dimension control achieved through varying the numerical aperture.

Exposure-defocus plots were generated based on aerial image modeling for an exposure tool with 193-nm wavelength, 0.5 NA, and 0.3- $\sigma$  illumination. The computer simulations were performed using Full Aerial Image Model [2] on a Silicon Graphics workstation. For these calculations, four different lenses were simulated. These lenses are referred to as lens 1 (ideal), lens 2 (excellent), lens 3 (mediocre), and lens 4 (poor), as defined by their Zernike polynomial coefficients used to describe lens aberrations. Table 3-1 lists these values for each of the lenses. Figure 3-1 shows the results for each of the four different lenses described in Table 3-1, where the y-axis was obtained assuming a 30% threshold and  $\pm 10\%$  exposure latitude. From this, it can be seen what effect various combinations of aberrations have on process window. In reality, a production lens might have aberration levels somewhere between lens 1 and lens 3, an area where there is significant overlap. Thus, we can conclude that the high image contrast realized by chromeless phase edges should be minimally affected by aberrations that might exist in a typical production lens.

The experimentally determined process window for our 193-nm, 0.5-NA, 0.6- $\sigma$  lens was measured. The resist process was a commercially available top-surface imaged silylation resist [3], slightly modified from the originally published baseline process [4]. Table 3-2 shows process conditions used for resist processing. The depth of focus is shown in Figure 3-2 and the exposure latitude is shown in Figure 3-3, where values are  $\sim 1.5\text{-}\mu\text{m}$  depth of focus and  $\sim 3\%$  exposure latitude, respectively. Although the depth of focus is near what is theoretically predicted for this lens, the exposure latitude is somewhat less. This, we feel, stems from scattered light originating in the projection lens and was exacerbated by the test reticle used, which was almost entirely bright field. Nevertheless, we feel that even this lens should be capable of limited 110-nm critical dimension demonstrations when combined with a proper reticle layout. The resolution limit of chromeless phase shifting masks exposed at 0.6  $\sigma$  is shown in Figure 3-4, as the line/space

**TABLE 3-1**  
**Lists of Zernike Polynomial Coefficients Used to Simulate**  
**Different Lenses for Aerial Image Calculations**

Aberration	Coefficient	Lens 1 (Ideal)	Lens 2 (Excellent)	Lens 3 (Mediocre)	Lens 4 (Poor)
90 Astigmatism	z5	0	0	0.01	0.02
45 Astigmatism	z6	0	0	0.01	0.02
90 Coma	z7	0	0.01	0.01	0.02
45 Coma	z8	0	0	0.01	0.02
Spherical	z11	0	0	0.01	0.02



*Figure 3-1. Exposure-defocus plots for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-numerical-aperture (NA), 0.3- $\sigma$  lens. The calculations were repeated four times for four different sets of lens aberrations.*

**TABLE 3-2**  
**Process Conditions for Modified Silylation**  
**Resist Processing**

Resist	MCC Nano MX-P7
Resist thickness	450 nm
Post-apply bake	100°C
Exposure dose	50–120 mJ/cm <sup>2</sup>
Silylating agent	DMSDMA*
Silylated depth	100 nm
Clearing dose	40 mJ/cm <sup>2</sup>
Etcher	Lam TCP 9400
Etch pressure	3 mT
Etch power, source	220 W
Etch power, chuck	100 W
Etch temperature	–30°C
*Dimethylsilyldimethylamine.	

period is decreased from 0.27 to 0.23  $\mu\text{m}$ . It is expected that slightly better resolution can be obtained at lower partial coherence.

We have also attempted to quantify lens distortions for the chromeless phase shifting mask. It has already been reported that isolated images printed with a 90° phase edge can actually be used to measure focal plane errors (i.e., field curvature) as well as both projection lens and illuminator aberrations [5]. In these cases, the image displacement is quantified by the magnitude of the image displacement per unit defocus, with values as large as 100 nm/ $\mu\text{m}$  not uncommon [5], and the largest displacements occur for low-coherence, on-axis imaging. Figure 3-5 shows simulation results for the four hypothetical lenses considered, where the image centerline position is plotted vs defocus. Even though the depth of focus for a ~100-nm line produced with a chromeless phase edge is large ( $>1 \mu\text{m}$ ), the image displacements as a function of defocus may be significant enough to limit the usable depth of focus, depending upon the magnitude of the aberrations, the partial coherence, and the overlay tolerance. In addition, these effects are

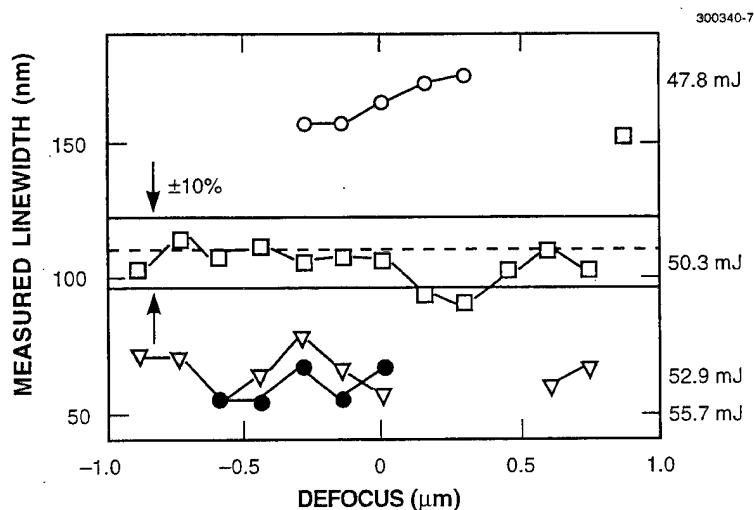


Figure 3-2. Experimentally measured focus latitude for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$  lens. The doses used were 48 mJ/cm<sup>2</sup> (open circles), 50 mJ/cm<sup>2</sup> (squares), 53 mJ/cm<sup>2</sup> (inverted triangles), and 56 mJ/cm<sup>2</sup> (closed circles). At a 50-mJ/cm<sup>2</sup> dose, the defocus latitude for a nominal 110-nm feature is  $\sim 1.5 \mu\text{m}$ .

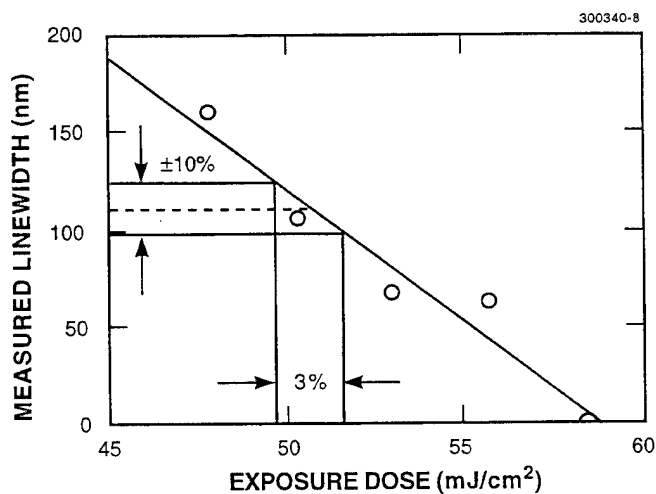
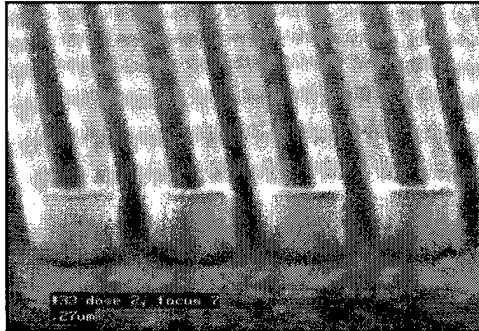
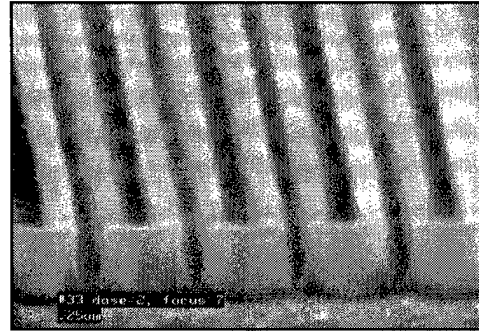


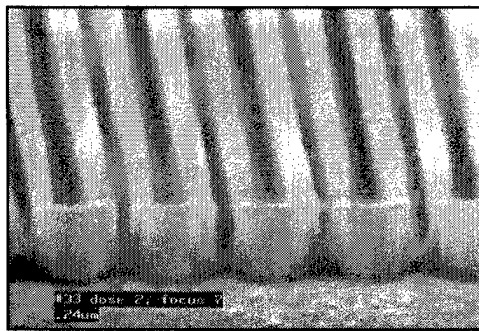
Figure 3-3. Experimentally measured exposure latitude for chromeless phase edge photomask used in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$  lens. The calculated latitude for  $\pm 10\%$  linewidth variation is  $\sim 3\%$  for a nominal feature size of 110 nm.



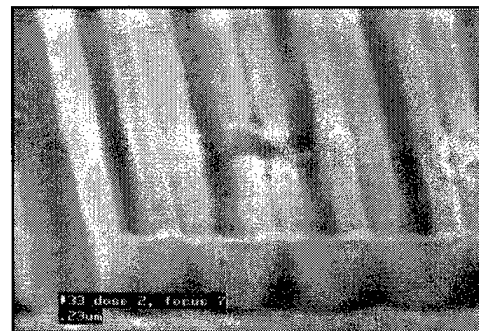
(a)



(b)



(c)



(d)

Figure 3-4. Electron micrographs of 110-nm isolated lines produced using chromeless phase edge photomask in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$  lens. The images show the change in feature profile as the spatial period is varied: (a) 270 nm, (b) 250 nm, (c) 240 nm, and (d) 230 nm.

additive to the aberration-induced displacements that exist at optimal focus. These displacements are most affected by coma, as illustrated in Figure 3-5, where lens 2 exhibits a z7 coma Zernike coefficient of 0.01, but has all other Zernikes set to zero.

Clearly, the absence of scalability of the magnitude of aberration- and focus-induced distortion represents a serious problem that must be overcome to successfully use chromeless phase shifting masked optical lithography at critical dimensions approaching the Rayleigh diffraction limit. However, additional potential problems exist for implementation of this technique. One obvious drawback with this approach stems from limitations in achievable geometry resulting from the “closed loop” nature of the etched phase edges; this limitation requires at least two exposures prior to resist development in order to obtain free-standing features. In the future, however, the perception that this characteristic represents a severe drawback may diminish as scanners capable of exposing 9-in. reticles come into use. This may allow for fast double exposures through placement of two virtual reticles on a single reticle plate, circumventing the need for cumbersome reticle loading and aligning between exposures.

One additional issue resulted from the use of low exposure doses. These doses were only  $\sim 1.1$  to  $1.4\times$  higher than the open frame dose  $E_0$  to resolve the 110-nm features, relative to  $\sim 2.1$  to  $2.4 \times E_0$  for dense features on a binary mask. We observed a subtle effect relating to increases in the amount of parasitic silylation as the exposure dose approaches  $E_0$ ; this effect is illustrated in Figure 3-6, where images are

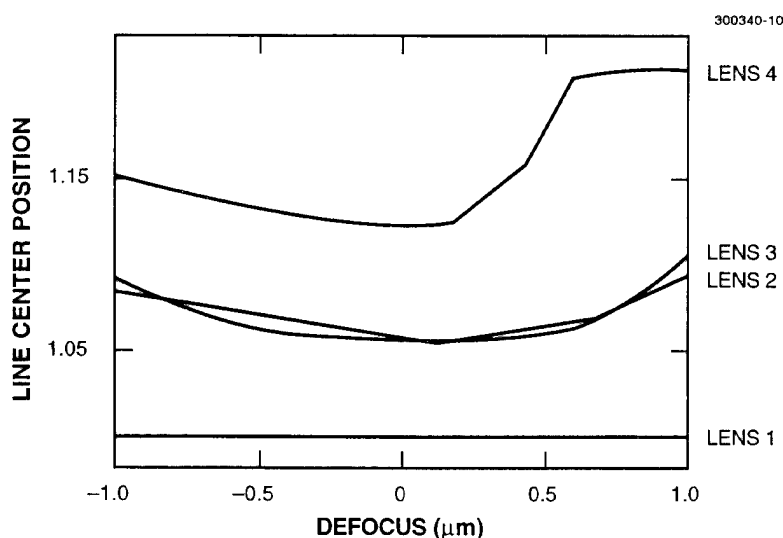
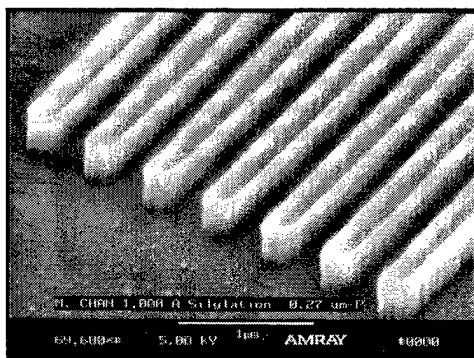
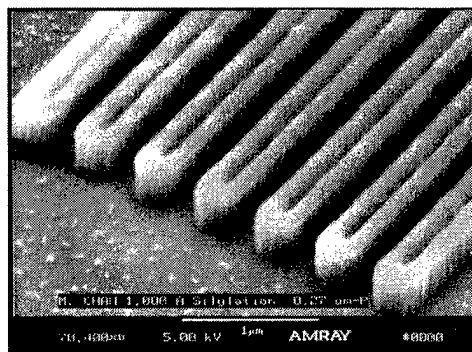


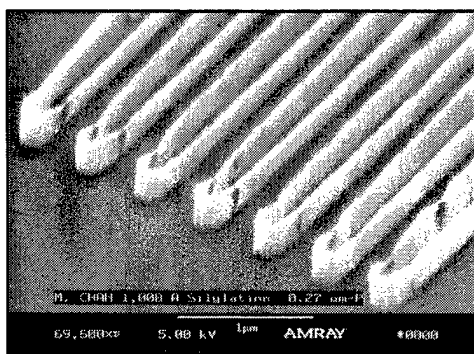
Figure 3-5. Aerial image calculations showing image placement for 110-nm isolated line vs defocus using four different sets of projection-lens Zernike polynomials. The image was created using a chromeless phase edge. The four lenses are described in Table 3-1.



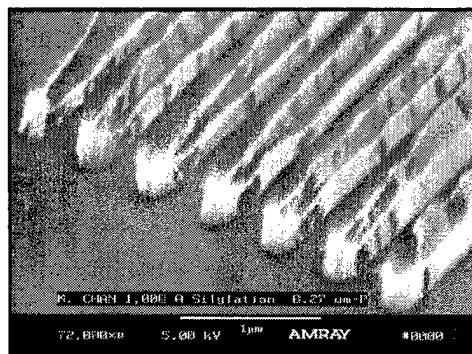
(a)



(b)



(c)



(d)

Figure 3-6. Electron micrographs of 110-nm isolated lines produced using chromeless phase edge photomask in conjunction with 193-nm, 0.5-NA, 0.6- $\sigma$  lens. The images show the change in feature profile as the exposure dose is varied: (a) 49 mJ/cm<sup>2</sup>, (b) 51.5 mJ/cm<sup>2</sup>, (c) 54 mJ/cm<sup>2</sup>, and (d) 58 mJ/cm<sup>2</sup>. Note the decrease in the amount of etch residue as the dose is increased.

shown at various doses. Note the decreased amount of parasitic silylation as the dose increases. This is a result of limited contrast in the silylation step, and should be less of a problem with a resist process possessing higher intrinsic contrast.

M. Chan	R. R. Kunz
S. P. Doran	M. Rothschild

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## 4. HIGH SPEED ELECTRONICS

### 4.1 DEVELOPMENT OF A SiC VERTICAL FIELD-EFFECT TRANSISTOR

An SiC-based vertical metal-semiconductor field-effect transistor (MESFET) is proposed which enables many performance advantages with respect to planar FETs. Its key feature is its submicrometer-periodicity U-groove grating structure. The submicrometer patterning is accomplished using interferometric lithography. The grooves are then etched using reactive ion etching (RIE). Interferometric lithography is a relatively unknown technique for producing very small features over wide areas, which we have used for many years for a variety of devices. Two laser beams are used to form a high contrast standing wave for exposing photoresist in a grating pattern, where the incident angle of the beams with respect to the substrate and the laser wavelength determine the periodicity of the grating. The exposed and developed photoresist is used to lift off a metal such as Cr or Ni, producing a metal grating on the wafer substrate.

Pattern transfer in single-crystal SiC requires the use of dry etching technology. In the RIE mode, we have obtained the high-resolution anisotropic etching required to produce the critical U-groove vertical structure for the proposed SiC power MESFET. Using Ni as a mask and  $\text{CF}_4$  as the etch gas at 10 mTorr and 250-V dc bias, we have obtained vertical sidewalls and smooth etched surfaces, as illustrated in Figure 4-1.

Figure 4-2(a) shows simulated current-voltage (I-V) characteristics for the device structure of Figure 4-1, but with the source and drain regions reversed (drain on top). Figure 4-2(b) shows the device I-V characteristics obtained by probing a few fingers of a partially drain-processed 6H SiC MESFET, but where the top ohmic contact is replaced by a forward-biased Schottky contact (the substrate ohmic is the source). The experimental device I-V curves exhibit the general shape predicted by the simulations. This result illustrates that transistor characteristics can be obtained with this structure and that they can be successfully modeled. Gate-to-substrate breakdown voltage was measured at 70–75 V.

More recently, similar drain-up characteristics have been obtained on a 4H SiC device wafer, and these are shown in Figure 4-3. We estimate the device active area to be  $10 \times 16 \mu\text{m}$ . Measured transconductance is near 20 mS (45 mS per millimeter of source finger width). Estimates of the intrinsic dc unity-current-gain frequency  $f_T$  obtained by measuring gate capacitance yield  $f_T = 15 \text{ GHz}$ . The higher transconductance and current apparent for the 4H device of Figure 4-3 compared to the 6H wafer of Figure 4-2 are, in part, due to the higher mobility of the 4H wafer. For source-up devices, we believe the difference between 4H and 6H devices will be somewhat smaller. These preliminary results are encouraging.

The preferred device configuration for the U-groove MESFET for most RF applications and all high-power switching applications is source on top (source up) which provides the best combination of power-frequency performance. This enables thicker drain-drift regions for high breakdown voltage  $V_B$ . Source-up devices have higher intrinsic  $f_T$ 's compared to the drain-up device because of the lower capacitance associated with removing the material on the source side of the device. The etched-groove structure also allows one to greatly minimize parasitic resistances on the source side of the device by controlling the

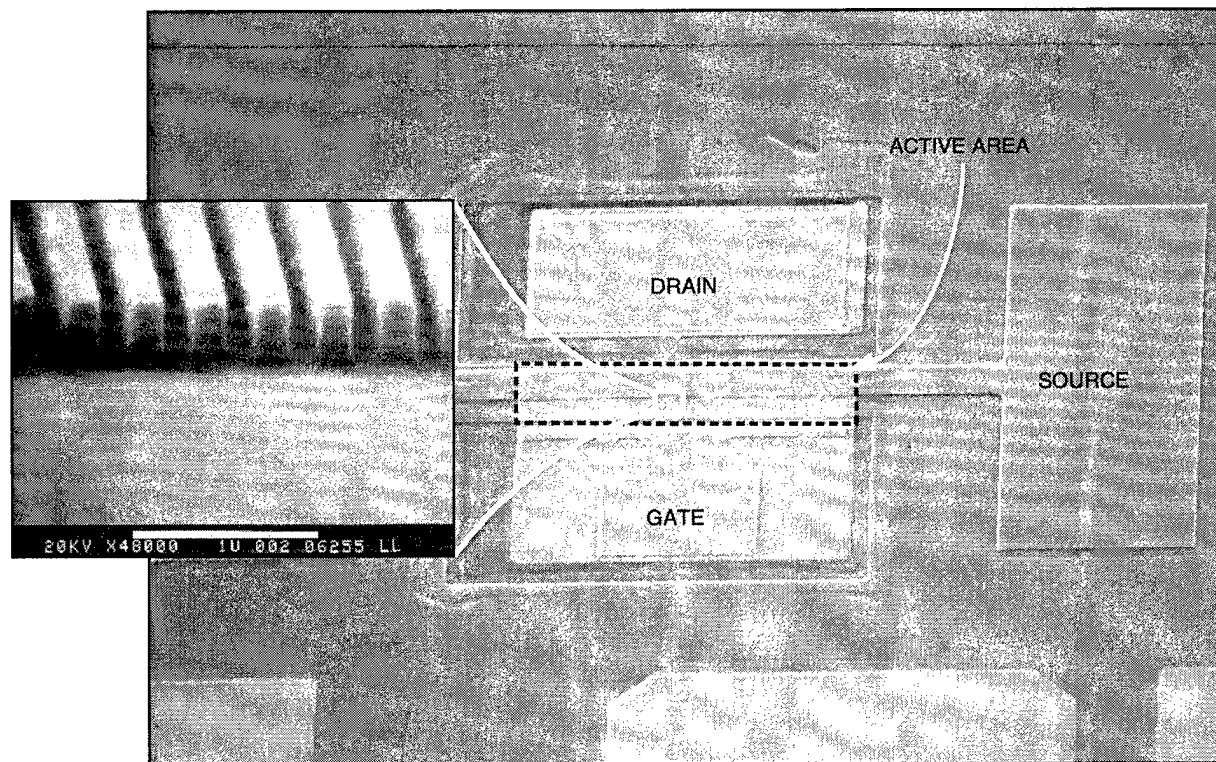


Figure 4-1. Scanning electron micrograph (SEM) of etched-groove grating structure in 6H SiC. The device active area ( $80 \times 16 \mu\text{m} = 4 \text{ mm}$  source width) is indicated by the dashed line.

gate-to-source length. Source resistance is the key parameter affecting measured device transconductance since it is reduced by the factor given below where  $g_m$  is the intrinsic transconductance and  $R_s$  is the source series resistance.

$$g_m(\text{observed}) = \frac{g_m}{1 + R_s \cdot g_m} \quad (4.1)$$

The top ohmic (source) contact is the most challenging aspect of the device fabrication sequence. This is because ohmic contacts in SiC presently require a high-temperature ( $>950^\circ\text{C}$ ) alloying step which

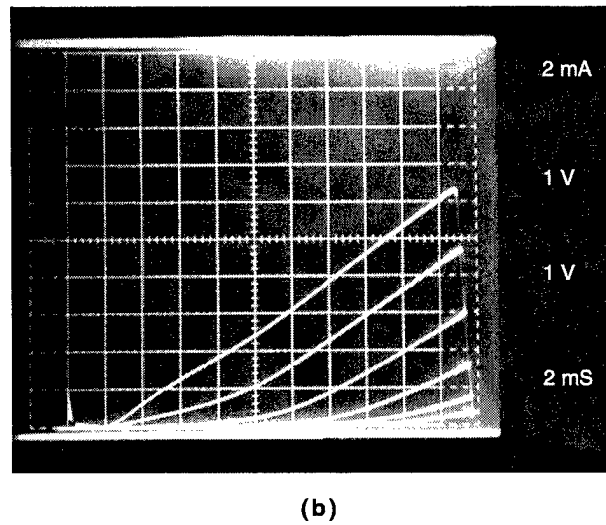
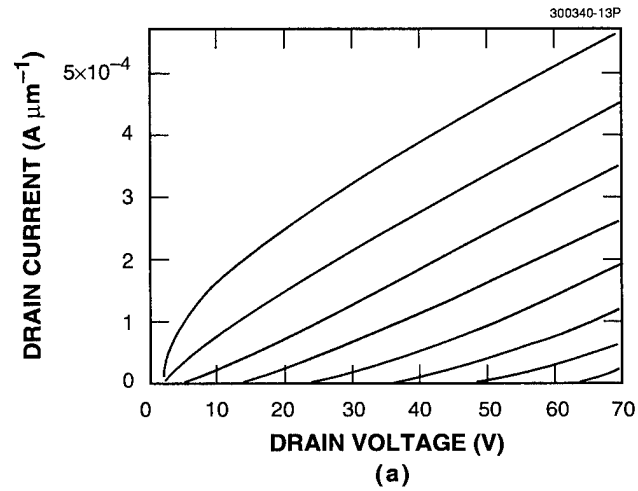


Figure 4-2. (a) Simulated and (b) experimental current-voltage ( $I$ - $V$ ) characteristics obtained for U-groove metal-semiconductor field-effect transistor (MESFET) structure of Figure 4-1, but with drain and source reversed. The top contact for the experimental device is a forward-biased Schottky drain with the substrate as the source.

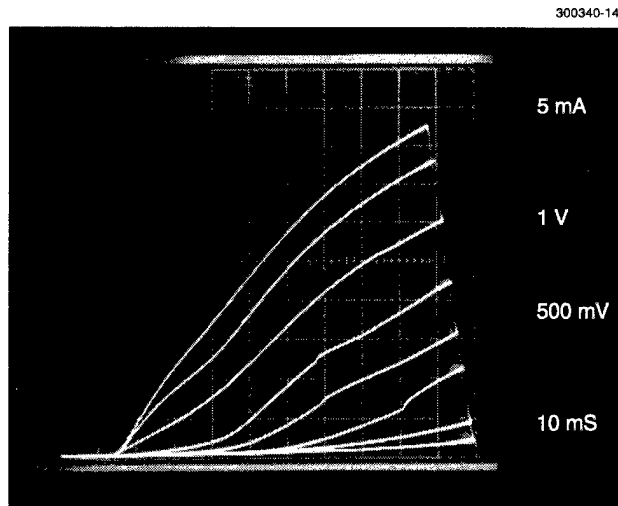
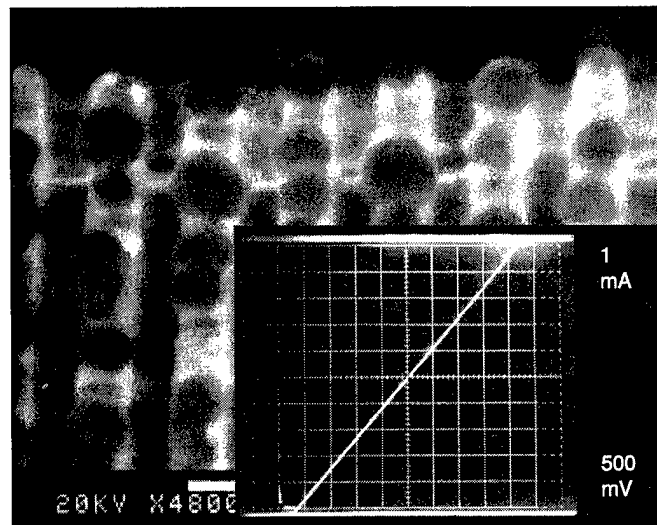


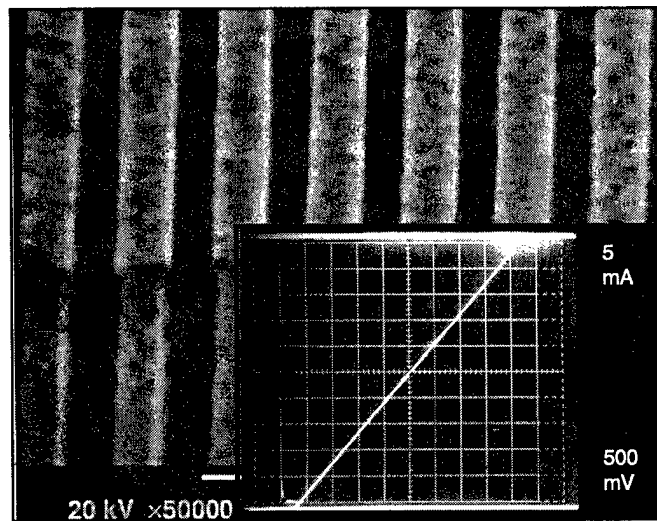
Figure 4-3. Characteristics of drain-up MESFET structure of Figure 4-1, but using 4H SiC. The distortions in the I-V curves are due to probe-induced oscillations.

would degrade the gate metal Schottky at the groove bottoms. Thus, the top ohmic contact must be formed before gate metallization. At present, we use glancing angle evaporations and lift-off to form Ni caps on the grating finger tops of the device active region. We are currently developing a self-aligned top ohmic process where Ni is first used as the grating RIE etch mask while the remaining Ni is alloyed directly into the top ohmic contact. In any case, the top ohmic contact is formed by alloying at temperatures in excess of 950°C. We have found a significant problem during early attempts to form this contact where the Ni appears to delaminate or ball up on the long, narrow (160 nm) grating fingers. This delamination greatly affects the integrity of the subsequent gate metal evaporation into the groove bottoms. Recently, we have developed a solution to this delamination effect through the use of a nitride cap to hold the Ni in place during the anneal. The results both physically and electrically are shown in Figure 4-4. The top ohmic I-V characteristics shown are obtained by probing between a number of adjacent grating fingers. We estimate that the total source-to-gate series resistance for a typical device will be on the order of 5–10  $\Omega$ .

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G. D. Johnson



(a)



(b)

Figure 4-4. (a) SEM of top ohmic after Ni alloying at 950°C, showing Ni delamination, and (b) SEM showing Ni after alloying at 1050°C but using nitride cap to prevent delamination. Insets show I-V characteristics of top ohmic probed between sets of adjacent fingers.

## 5. MICROELECTRONICS

### 5.1 128 × 128-PIXEL CCD IMAGER WITH JFET READOUT AMPLIFIERS

Epitaxially grown *p*-channel junction field-effect transistor (JFET) devices, used to convert charge packets into a voltage signal, have been successfully integrated onto a 128 × 128-pixel charge-coupled device (CCD) imager. The joint fabrication demonstrates that the process sequence used to form the JFET structure is compatible with CCD imager manufacture. The JFET devices are being added to the CCD imager in an attempt to reduce the noise added to the signal during the charge-to-voltage conversion step. This report describes the integration of the JFET with the CCD imager and also gives the JFET readout amplifier performance.

The 128 × 128-pixel CCD imager has a frame-transfer architecture and is fabricated using a three-layer polysilicon/single-layer metal process [1]. The CCD imager has four readout ports with one amplifier associated with each 32 × 128-pixel section of the imaging array. The readout amplifier consists of two JFET devices used in a source-follower configuration. Figure 5-1 is an optical photograph showing the JFET devices as well as a portion of the CCD output register. The source-follower load transistor has width × length of 13 × 14 μm while the sense transistor has dimensions of 7 × 7 μm.

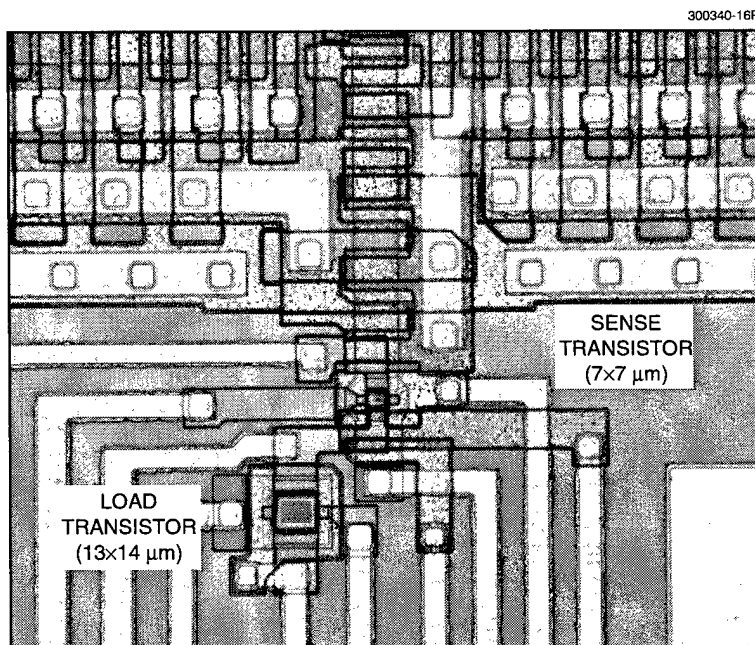


Figure 5-1. Optical photograph of the junction field-effect transistor (JFET) source-follower amplifier at end of charge-coupled device (CCD) output register.

The imager fabrication begins by using the conventional CCD process. After deposition, etch, and oxidation of the third polysilicon layer, the process deviates from the CCD fabrication sequence to create the JFET structures. The JFET devices are formed in spaces that have been intentionally left between two polysilicon gate electrodes. The oxide/nitride/oxide layers created in the CCD process are removed from this region, and a silicon layer is epitaxially grown from the newly formed seed holes. The JFET source and drain regions are formed by ion implantation into the epitaxial silicon. After a thermal oxidation that grows approximately 1200 Å, an  $n^+$  back gate is created by etching holes in the oxide and depositing an  $n^+$  polysilicon layer. Processing is completed using the conventional CCD sequence to open the contacts and define the metal. Figure 5-2 shows cross-sectional and top views of the finished JFET device and CCD gate electrodes. A more detailed description of the process and JFET device operation is given in Ref. 2.

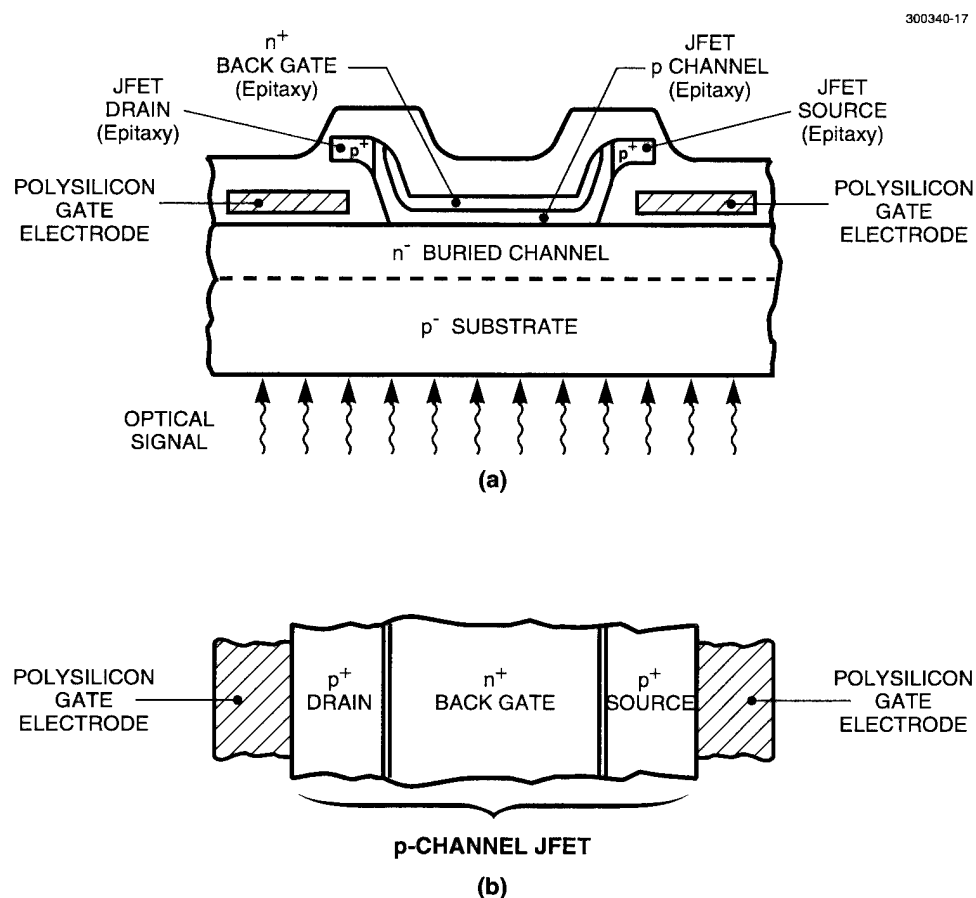


Figure 5-2. (a) Cross-sectional and (b) top views of finished JFET device with surrounding CCD gate electrodes.

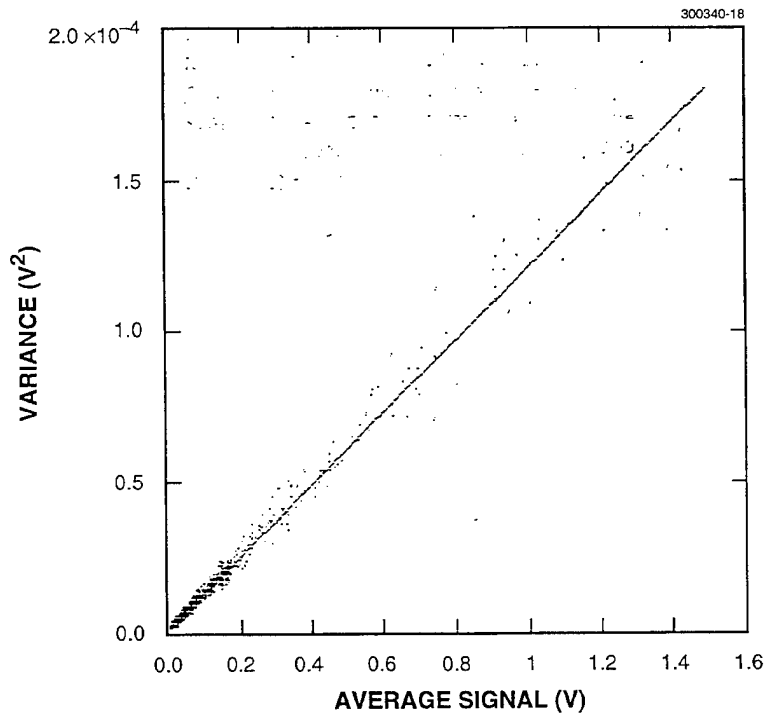


Figure 5-3. Average signal vs variance for each pixel in  $32 \times 128$ -pixel section of imaging array. The voltage gain and bandwidth for the measured data were 22 and 5 MHz, respectively.

Fully functional CCD detectors with all four readout amplifiers working were successfully fabricated. The responsivity (charge-to-voltage conversion factor) and readout amplifier noise were measured on the finished CCD imagers. The photon transfer technique [3], which employs the average signal and corresponding standard deviation (or variance), was used to extract these parameters. Figure 5-3 is a plot of the average pixel signal vs the variance. The data in the curve are created by nonuniform illumination of the CCD imaging array. Each point displayed in these curves represents one pixel in a  $32 \times 128$ -pixel section of the imaging array, and the result for an individual pixel is an average value calculated from 400 image frames. The slope of the curve is equal to two times the square of the responsivity and voltage gain. The responsivity extracted from the slope has a value of  $4.5 \mu\text{V}/e$ . The noise of the readout amplifier is calculated from the intercept where the intercept is two times the noise (in electrons) multiplied by the square of the responsivity and voltage gain. The readout noise using the intercept is calculated to be approximately 13 to 14 electrons.

The performance of the JFET amplifiers can be compared to the conventional floating diffusion amplifier used on most CCD imagers. The responsivity and noise of Lincoln Laboratory's floating diffusion amplifier is  $25 \mu\text{V}/e$  and 4 to 6 electrons, respectively. The higher noise and lower responsivity of the JFET amplifier are caused by parasitic capacitance between the charge packet and JFET source. Process and design modifications have been developed that should improve the JFET performance beyond that of the floating diffusion amplifier.

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McD. Robinson*	E. D. Savoye
D. J. Young	

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## 6. ANALOG DEVICE TECHNOLOGY

### 6.1 2-GHz OPERATION OF THE DIGITAL CONTROL REGISTERS OF A PROGRAMMABLE FILTER FOR A SPREAD-SPECTRUM MODEM

In a recent report we described the architecture of the programmable filter for a superconductive direct-sequence spread-spectrum modem designed to operate at a chipping rate of 2 gigachips per second, and we reported test results on the digital subcircuits of the filter [1]. The chips tested at that time consisted mostly of individual subcircuits and pairs of connected subcircuits to allow for complete characterization of those circuits and their interfaces. The chips also contained a seven-stage prototype filter, but the limited number of pins available on a chip made it impossible to provide connections to all of its inputs and outputs. We have now designed a new mask set containing completely wired prototype filters, and we have operated the digital control registers at speeds up to 2 GHz using data patterns of the type that would be used during the operation of the filter.

A high-level block diagram of the filter is shown in Figure 6-1. The upper section shows a bank of analog T/H cells (the analog data register) and a digital shift register (the sampling control register). This shift register is loaded with all 0's except for a single 1, which serves as an index. Where the 1 appears, the corresponding T/H cell takes a new sample. This 1 circulates through the shift register, causing successive

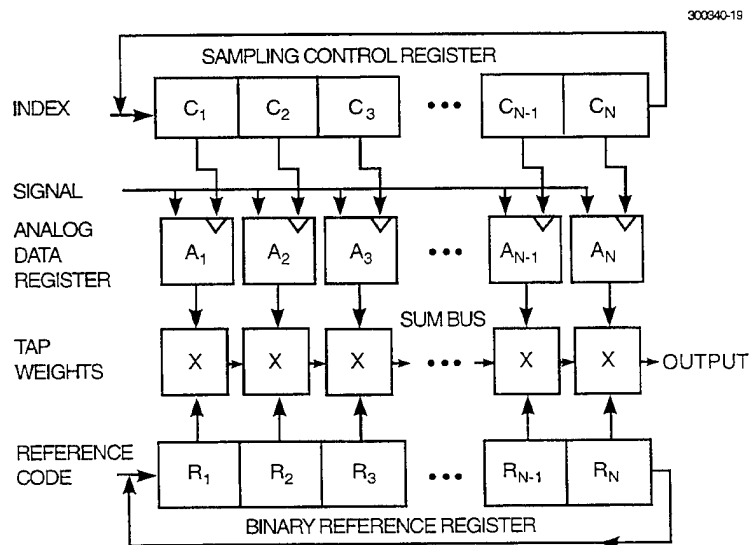


Figure 6-1. Block diagram of superconductive programmable matched filter.

analog samples to be taken in successive T/H cells. Thus, at any given time the most recent  $N$  samples of the input signal are stored in the analog data register, with the newest sample at the index, with progressively older samples to the left and wrapping around to the right, and with the oldest sample just to the right of the index.

The lower section of the block diagram shows a bank of tap-weight cells and another shift register (the binary reference register), which is loaded with a time-reversed copy of the code that was used in the transmitter to spread the signal. Each tap multiplies the analog sample stored in the corresponding T/H cell by either +1 or -1 (or, alternatively, +1 or 0) depending on the bit stored in the reference register. As the two shift registers are clocked synchronously, the reference code moves past the stationary samples of the

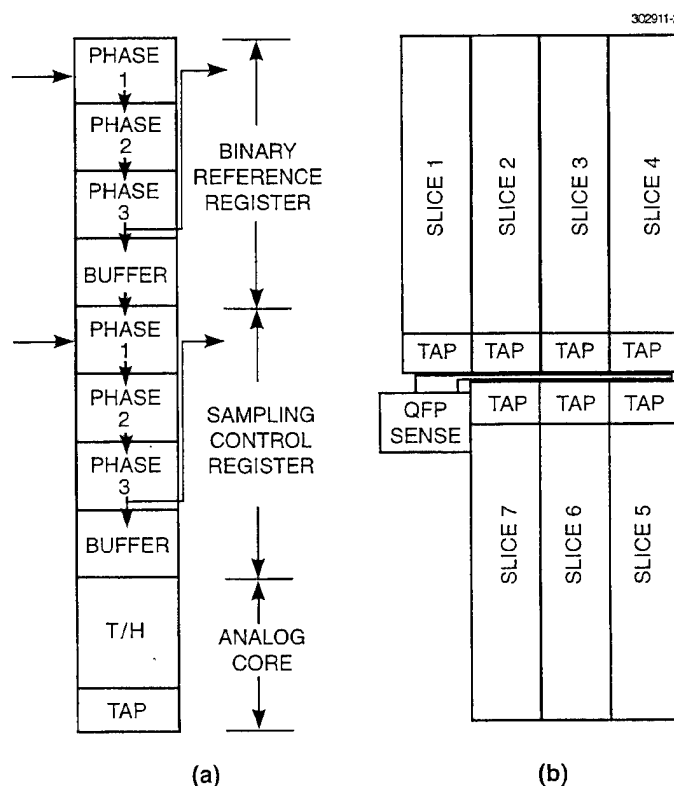


Figure 6-2. Filter comprising mainly an array of identical elements, one for each bit in the spreading code: (a) block diagram of element, referred to as a slice; and (b) arrangement of slices to form seven-stage filter. A wire that runs by and couples inductively to each tap serves as a summing bus, whose signal is connected to a quantum flux parametron (QFP) sense circuit.

input signal. When the reference code aligns with the received signal, a correlation peak occurs. The output signal peaks strongly in a positive direction for an encoded signal bit of 1 and in a negative direction for a signal bit of 0.

For each bit (or "chip" in spread-spectrum terminology) of the spreading code, the filter contains an identical section called a slice, a block diagram of which is shown in Figure 6-2(a). The topology of the slice differs from the arrangement shown in the block diagram in that the analog and digital components are segregated, the former to the bottom and the latter to the top of the slice. This is done to minimize parasitic inductances in the analog circuitry. The slices are arranged to form the filter, as shown in Figure 6-2(b), so that an inductive summing loop can couple to all of the tap elements with a minimum of stray inductance. For the same reason, the slice is kept very narrow, with the gates of the three-phase shift registers and the buffer stacked vertically. The output of the buffer in the sampling control register drives the T/H, which is directly below it. The buffer from the binary reference register has to snake by the other circuitry to reach the control input to the tap circuit.

Because the complete prototype filter is too large and complex to show with useful resolution in a single figure, we focus on two subsections. Figure 6-3 is a plot from the layout software that illustrates the top part of the filter, which includes the first four stages of the binary reference register. Figure 6-4 shows a plot of the analog core section of all seven stages plus the summing bus and the quantum flux parametron output comparator. To reduce clutter in the figures, only three layers of the doubly planarized all-refractory technology for superconductors (DPARTS) process are shown: M2 (base-electrode metal), M4 (wiring metal), and R1 (resistors). The circuit layers not shown are M3 (counterelectrode), M5 (ground-plane metal), I2 (vias through the oxide between M2 and M4), and I3 (vias through the oxide between M4 and M5).

The most complex test of the prototype filter performed thus far was the simultaneous operation of both shift registers with high-speed waveforms of the type that would be used in full operation. A 1-GHz word generator with return-to-zero (RZ) outputs provided the input signals to the shift registers. Figure 6-5 shows the screen of a Tektronix sampling oscilloscope during the experiment. The input to the binary reference register was a repeating 15-chip pseudo-noise (pn) code, while the input to the sampling control register was a single index pulse once per 15-chip cycle. The time delays between input and output signals are largely determined by the lengths of the cables to the oscilloscope, which were not matched. Thus, there is no significance to the absolute timing of any of the signals shown. The results demonstrate that the digital components in the filter were fully functional at high speed.

By combining two 1-GHz RZ word-generator output channels with a 500-ps phase shift between them, a 2-GHz non-return-to-zero (NRZ) waveform was produced and used to test each shift register at full speed. Figure 6-6 shows the waveforms captured during that experiment. The two channels of the word generator were programmed with alternating chips of the 15-chip pn code so that, when combined, they

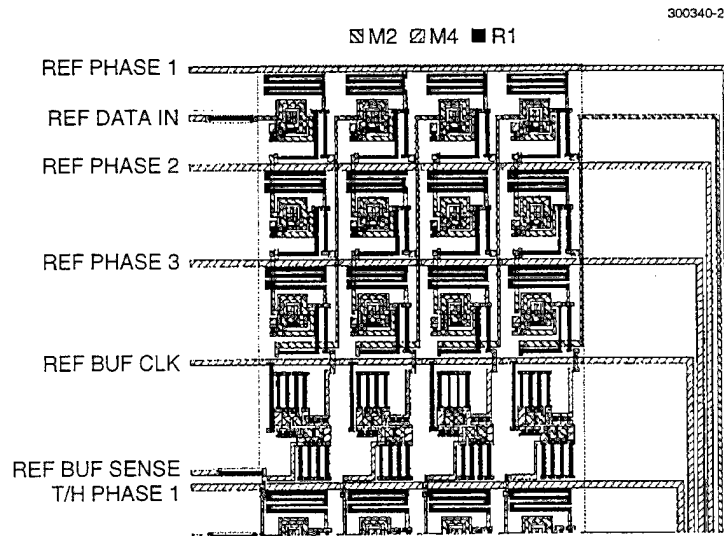


Figure 6-3. Layout of top part of prototype test filter, showing three-phase shift register and buffer array that constitute binary reference register.

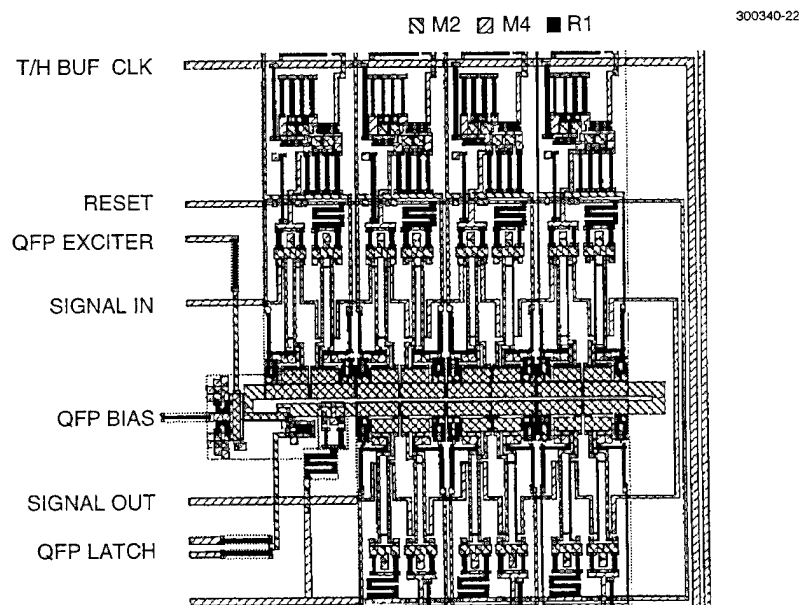


Figure 6-4. Layout of analog core section of prototype filter. At the top one sees the buffers of the sampling control register. The T/H elements, with the input signal applied, are seen above and below the taps, with the summing bus connected to the QFP sense comparator.



*Figure 6-5. Waveforms captured during simultaneous operation of both shift registers in filter at 1 GHz with return-to-zero (RZ) input signals. The horizontal scale is 5 ns per division. The top trace shows one phase of the 1-GHz sine wave clocks. The second and third traces show, respectively, the input to and output from the binary reference register, while the bottom two traces show, respectively, the input to and output from the sampling control register.*

produced an NRZ version of the same code shown in Figure 6-5. Thus, functionality at the full design speed was established.

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D. A. Feld

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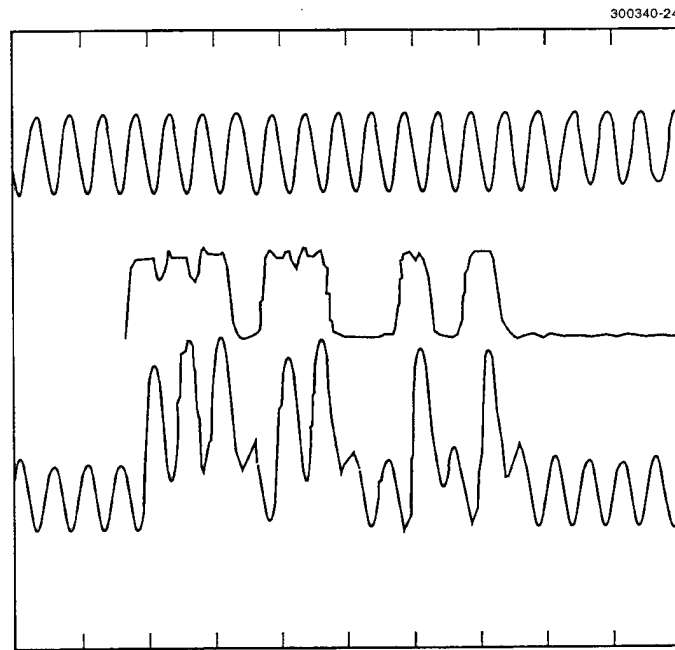


Figure 6-6. Waveforms captured during operation of single shift register at 2 GHz using non-return-to-zero input signal produced by combining two 1-GHz RZ channels from the word generator. The horizontal scale is 1 ns per division. The top trace shows one phase of the 2-GHz sine wave clocks. The second and third traces show, respectively, the input to and output from the binary reference register.

## 7. ADVANCED SILICON TECHNOLOGY

### 7.1 3.2 G-SAMPLE/SECOND SILICON-ON-INSULATOR CMOS DATA THINNER FOR A SUPERCONDUCTIVE COMPRESSIVE RECEIVER

An earlier report described the successful operation of a test chip containing the kinds of digital circuits suitable for a data thinner of a superconductive compressive receiver [1]. The next step has been the design of the high-speed portion of an actual data thinner. It is called the DCOP test chip after the main computation it performs, digital center-of-pulse detection. The design has been completed, and the chip is being fabricated at Lincoln Laboratory in a fully depleted silicon-on-insulator (SOI) CMOS process with  $0.25\text{-}\mu\text{m}$  transistor gates. It contains 22 000 transistors. A block diagram of the DCOP test chip is shown in Figure 7-1, and an annotated plot of the metal 1 mask layer is shown in Figure 7-2.

In the superconducting compressive receiver, incoming signals are mixed with a swept local oscillator and then passed through a chirp filter made from a superconducting tapped delay line. Continuous frequencies in the input signal emerge as compressed pulses, where the delay of the pulse relative to the start of the sweep is a linear function of the incoming signal's frequency. The chirp filter output is envelope detected, log amplified, and then sampled at 3.2 G-samples/second. Four samples in parallel ( $X$  in Figure 7-1), each six bits, are clocked at 0.8 GHz onto the DCOP test chip. The function of the chip is to locate the pulses among the input samples, in the presence of random noise and the sidelobes surrounding other pulses. An additional channel of four parallel six-bit samples ( $X_{inh}$  in Figure 7-1) can be used as a threshold to suppress the detection of pulses at certain sample positions.

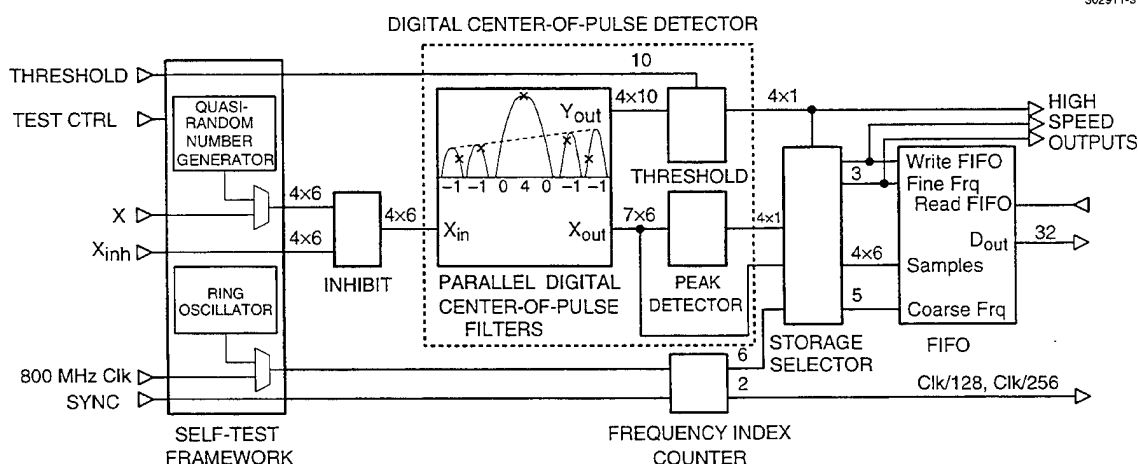


Figure 7-1. Block diagram of digital center-of-pulse (DCOP) test chip.

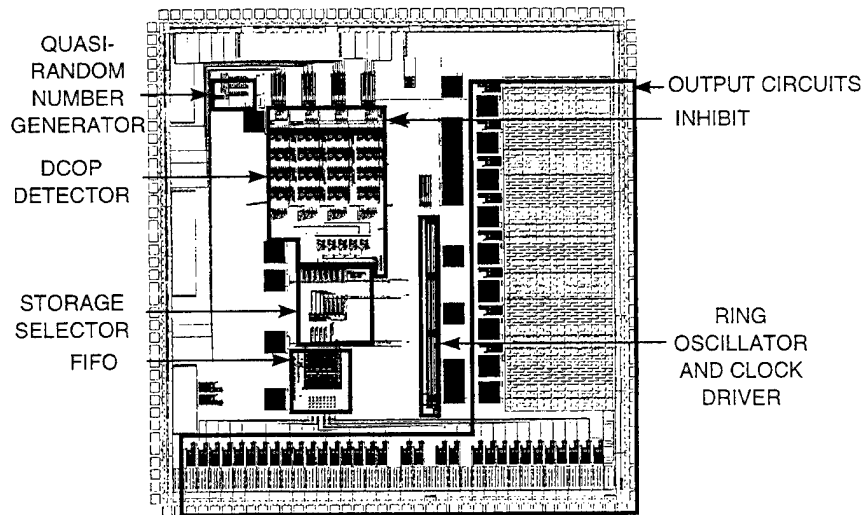


Figure 7-2. Metal 1 plot of DCOP test chip.

The self-test framework allows the chip to be operated in two different modes. In the normal mode the  $X$  and  $X_{inh}$  signals and an 800-MHz clock are supplied externally. In the test mode the clock is provided by an on-chip, tunable ring oscillator, and the  $X$  samples by an on-chip quasi-random number generator. The  $X_{inh}$  inputs are held at some fixed value during such testing. The test mode allows the functionality of the chip to be checked with a wafer prober too slow to supply 800-MHz signals. In both the normal and test modes, information describing the detected pulses is stored in the FIFO. In the DCOP test chip the FIFO can later be read out to the output pins. In a future application-specific integrated circuit (ASIC), which will be used in a brassboard version of the compressive receiver system, the FIFO will supply an on-chip bank of signal trackers, clocked at ~100 MHz, that will further reduce the data rate to the point where it can be handled by off-the-shelf digital signal processors.

The heart of the DCOP test chip is the DCOP detector itself (dashed box in Figure 7-1). On each clock four samples  $X_{in}$  enter the parallel DCOP filter, and four filter values  $X_{out}$  are produced. Each sample enters, on successive clocks, five out of the sixteen 10-bit adder/subtractors in the filter bank. For each incoming sample  $x_n$ , the filter bank computes

$$y_n = -x_{n-3} - x_{n-2} + 4x_n - x_{n+2} - x_{n+3} \quad (7.1)$$

Note that the samples immediately before and immediately after  $x_n$  are not used by the filter. The excluded samples are the ones most likely to fall within the error sidelobes of a pulse. The picture inside the filter box in Figure 7-1 shows a pulse (center) among the sidelobes of a nearby, and much larger, pulse. The sample values are marked by  $\times$ . If one calls the central sample  $x_c$ , then  $y_c$  will be positive, whereas the values  $y_{c-2}$ ,  $y_{c-1}$ ,  $y_{c+1}$ , and  $y_{c+2}$ , for example, will be negative. The same would be true if the noncentral samples represented random noise rather than sidelobes.

The usefulness of the DCOP filter is that it permits samples falling on pulses to be separated from the other samples by a threshold operation on  $y_n$  using a uniform threshold value that works over a wide dynamic range of pulse amplitude. This has been demonstrated by simulation with a variety of anticipated sample waveforms. Had one to choose a single threshold to apply to the raw sample data  $x_n$ , it would have to be much higher to avoid false alarms from the sidelobes of large pulses, and then the smaller pulses would not be detected, i.e., the dynamic range would be less.

The choice of which sample to call the peak sample of a compressed pulse requires both the thresholded output of the DCOP filter and the output of a simple peak detector, which finds a local maximum in the sample sequence. The filter output alone is insufficient, because it is possible for more than one sample on a compressed pulse to give a filter output above threshold. The peak detector alone would choose every peak of random noise in-between the real pulses. The storage selector uses the logical AND of the DCOP filter and peak detector outputs to choose the sample corresponding most closely to the actual peak frequency. The future ASIC will have a frequency interpolator that can use a few samples around a peak to refine the frequency to a value between those frequencies corresponding exactly to the samples. The frequency index counter is started at zero when a new sweep starts and counted up by four on each clock. It provides all but the two least significant bits of the frequency index, which are supplied by the storage selector according to which of the four samples for that clock period was chosen as the peak sample. The peak sample, the previous sample, the two following samples, and the frequency index are stored as a 32-bit word in the FIFO.

There is logic in the storage selector to handle the case where there are two pulses within a single clock time. This could occur if there were two closely spaced frequencies in the receiver input. Since the FIFO can store only one set of peak information in one clock period, the extra peak's information is kept until it can be stored in the next clock period. Too many closely spaced pulses will eventually cause information to be lost.

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## REFERENCES

1. Solid State Research Report, Lincoln Laboratory, MIT, 1996:4, p. 41.

# REPORT DOCUMENTATION PAGE

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